



A790GXM-AD3 V : 1.0

REVISION HISTORY:

Rev Date

Notes

SCHEMATICS TABLE:

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A---25/07/08 - 15-V18-010010

B---15/10/08 - 15-V18-010020

1.0 --- 01/07/09' --
15-V18-011000(GE1)
15-V18-011001(CHUANYI)

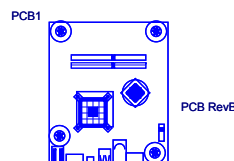
1. From V17100(RS780DM-A)
2. Change to AM3 CPU&DDR3
3. Add e-SATA
4. Add Stand-By LED
5. Add NBFAN*1
6. DEL COM1& Add DVI
7. Add CLR_CMOS Button
8. Del 1394
1. Modify for scrool/flighting screen
2. Increase stability issue
3. Verify audio connector & EMI suggestion
4. Move NB_FAN&PWR_FAN placement & cost-down some Ohm parts
5. Change PCB silkscreen with PWR_BTN&RST_BTN + SATA1~SATA6
6. Revise eSATA circuit
7. SB ver. from A12 change to A14(PA_SB700AJ8)
1. Modify for scrool/flighting screen
2. Increase stability issue
3. Debug HDMI (EMI) suggestion
4. SB Ver. Change from A14 to A12
5. SATA1/2~SATA5/6 Refine
6. Revise OS-CON to E/C
7. SB ver. from A12 change to A14(PA_SB700AJ8)

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Notes:

- 1). "PWR" net means inner power plane under impedance trace.
- 2). "GND" net means inner ground plane under impedance trace.
- 3). IP1 footprint is J2X2_IP
- 4). After nelist running, please specially take care the single net name: "IMPEDANCE_T" and "IMPEDANCE_B".



PCB Impedance control

Impedance (OHM)	Trace Width (mil)	Trace Length (inch)	Pre-preg	Default
50	4 (20/4/20)	8	1080	V

1)Circuit type 1

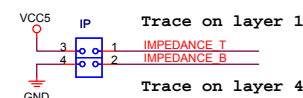
Layer 1:TOP

Layer 2:PWR

Layer 3:GND

Layer 4:BOTTOM

PCB STACK:



IMPORTANT NOTES ABOUT THIS SCHEMATIC

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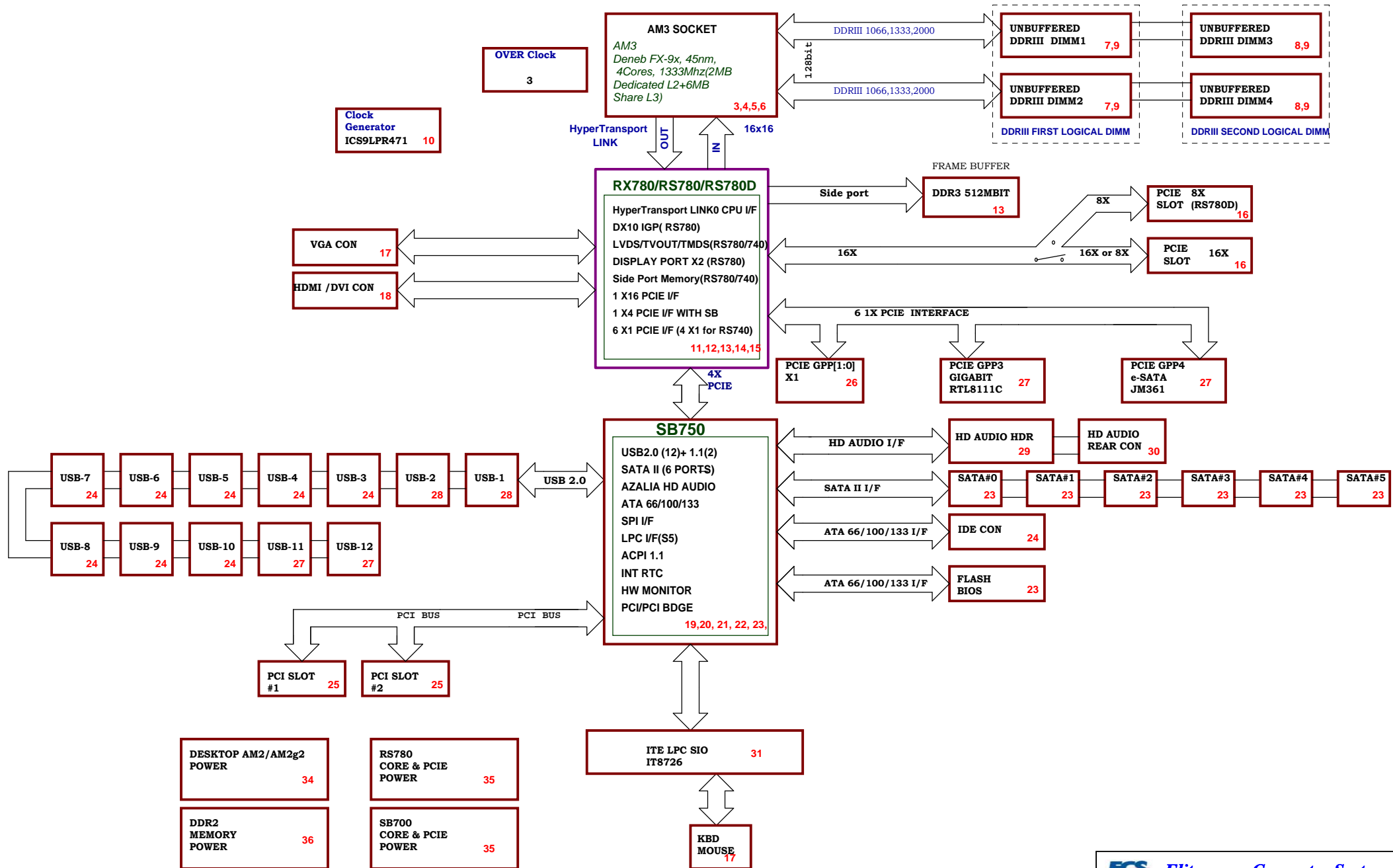
1) DESIGN NOTES in grey are information notes.

DESIGN NOTE: Example text for the design note to show the note inside the colored box.

2) DESIGN NOTES in yellow are notes of caution.

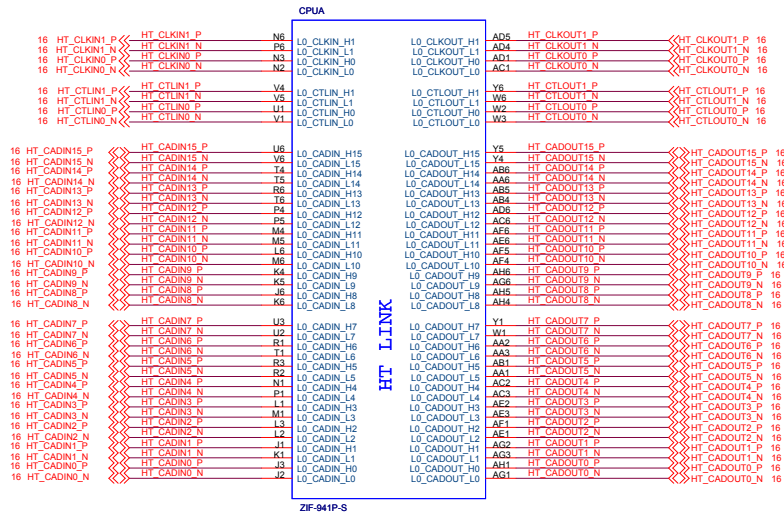


3) DESIGN NOTES in red are critical, and must be understood and followed.

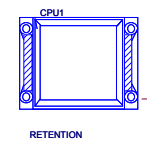
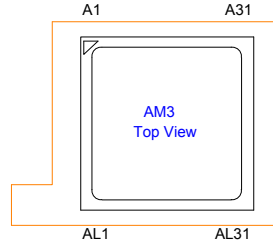


CPU HyperTransport and Overclock

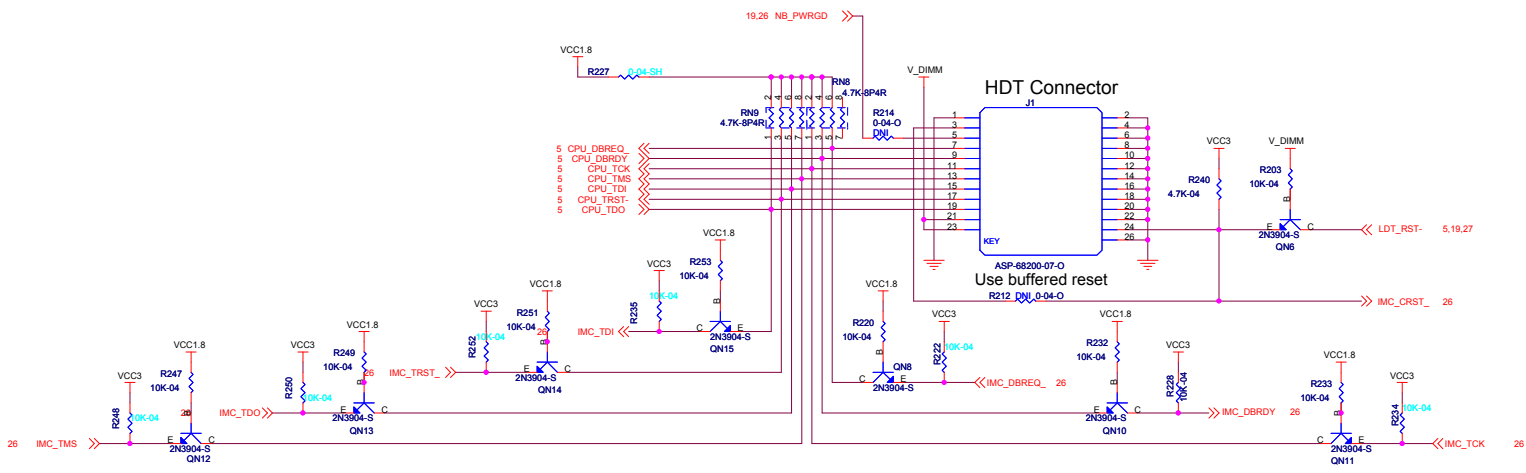
HyperTransport



Please use 1mm pad size,
place all ELT test pads
on bottom side only.



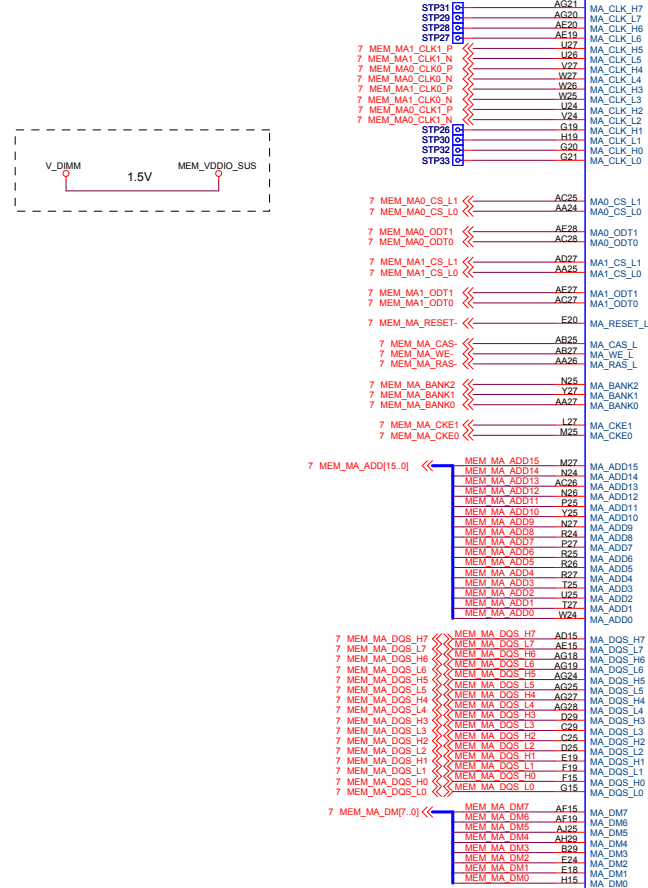
Over Clocking



CPU Memory

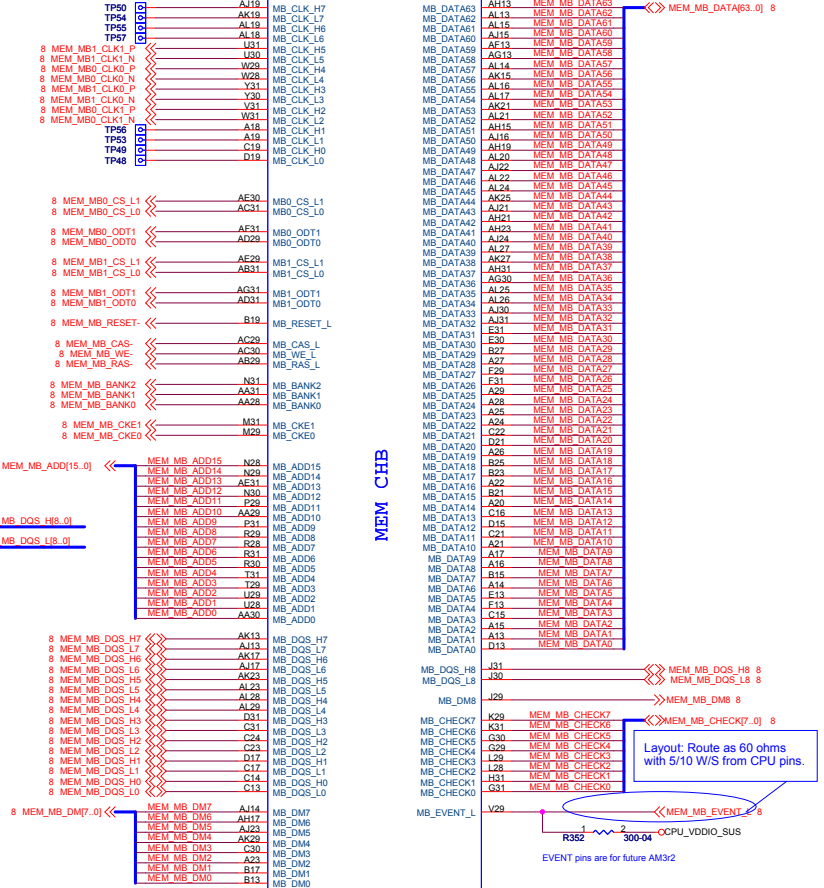
DDR3 Memory Interface A

Pin naming for memory pins indicate
"DDR3"/"DDR2" connections.



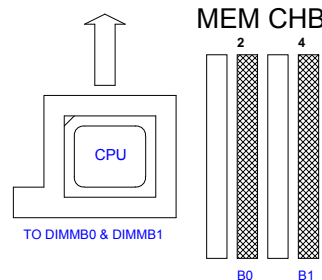
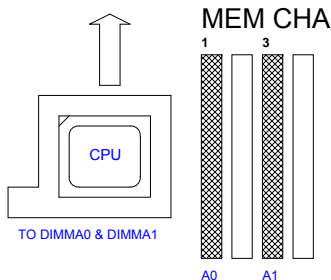
DDR3 Memory Interface B

Pin naming for memory pins indicate
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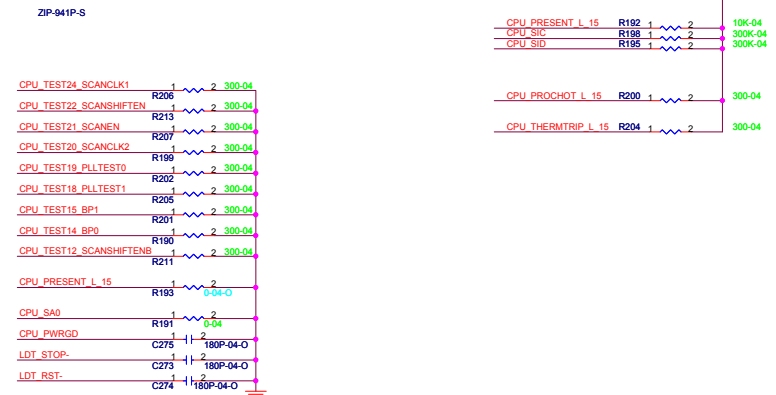
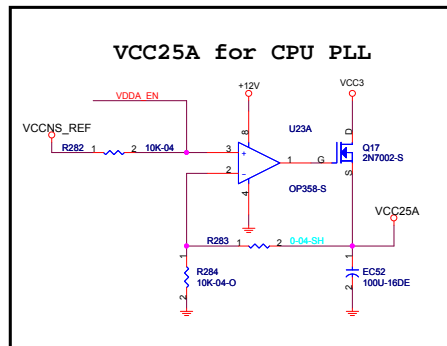
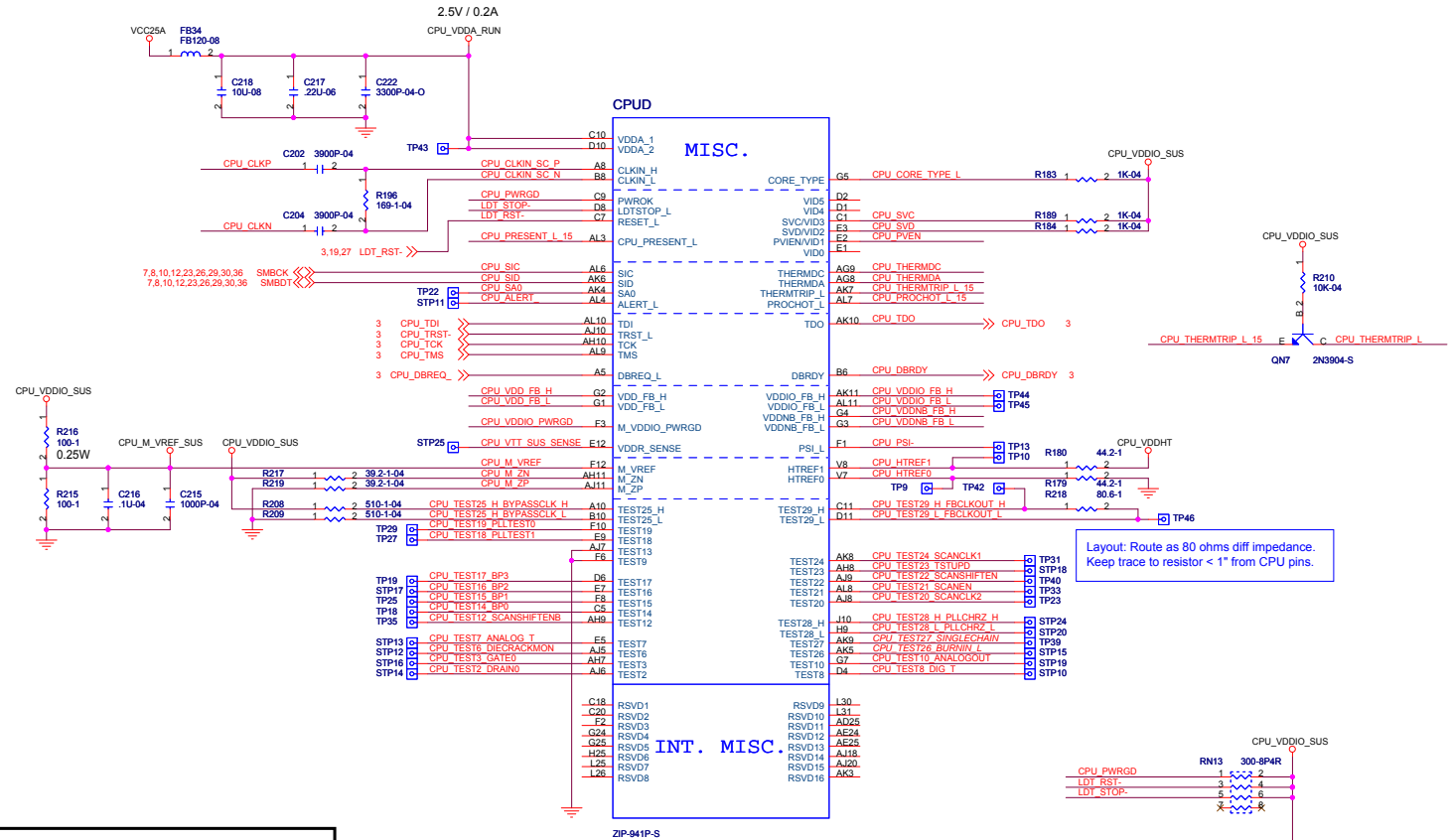
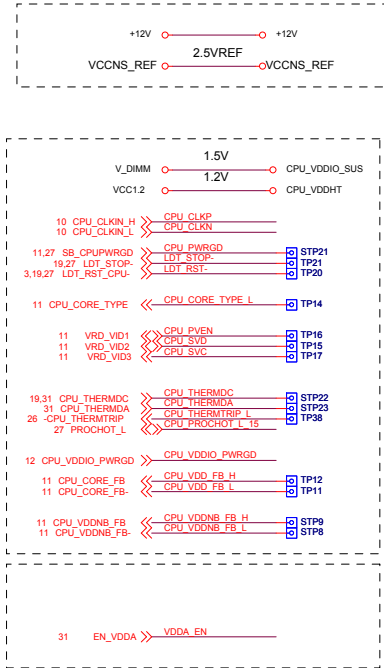


MEMORY CLOCK TRANSLATION

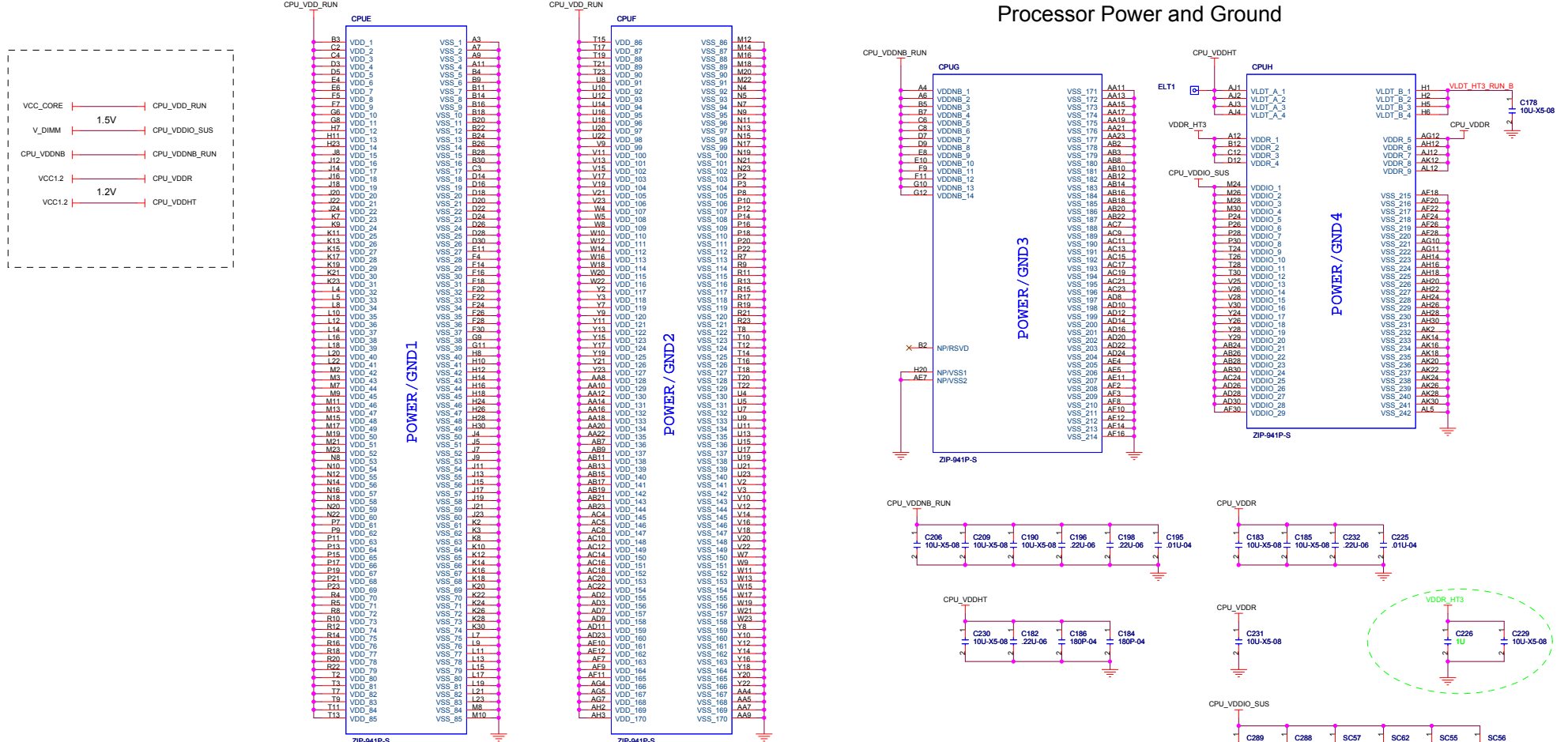
DIMM	DDR3 Memory Signal	CPU Signal
DIMM A0	MEM_MA0_CLK1 MEM_MA0_CLK0	MA_CLK2 MA_CLK4
DIMM A1	MEM_MA1_CLK1 MEM_MA1_CLK0	MA_CLK5 MA_CLK3
DIMM B0	MEM_MB0_CLK1 MEM_MB0_CLK0	MB_CLK2 MB_CLK4
DIMM B1	MEM_MB1_CLK1 MEM_MB1_CLK0	MB_CLK5 MB_CLK3



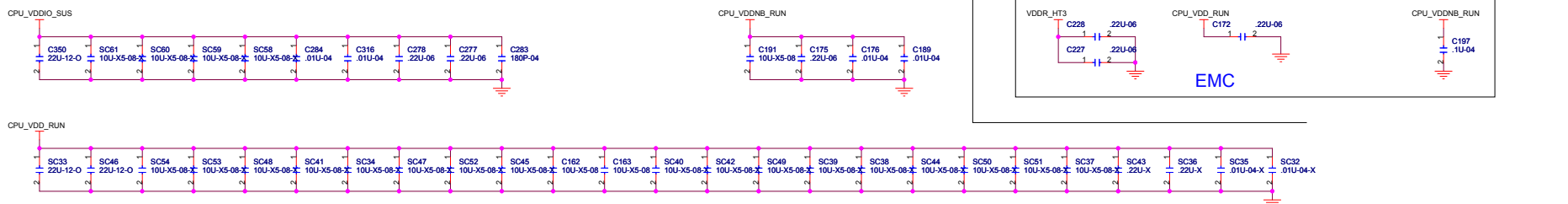
CPU Control and Miscellaneous



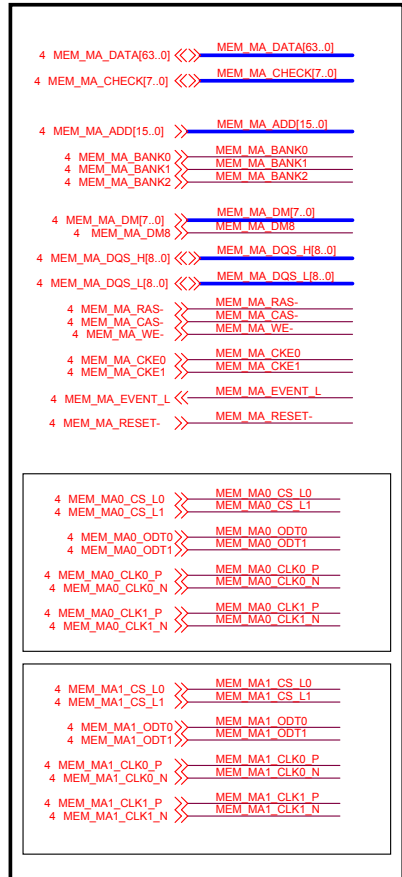
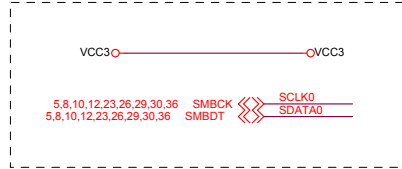
Processor Power and Ground



Bottom Side Decoupling

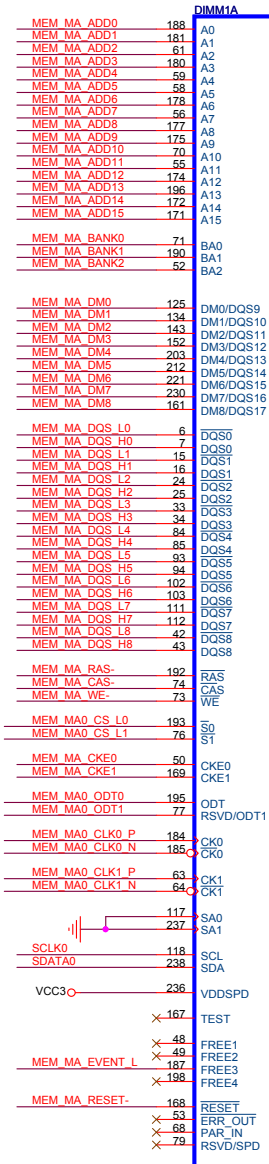


A Chanel

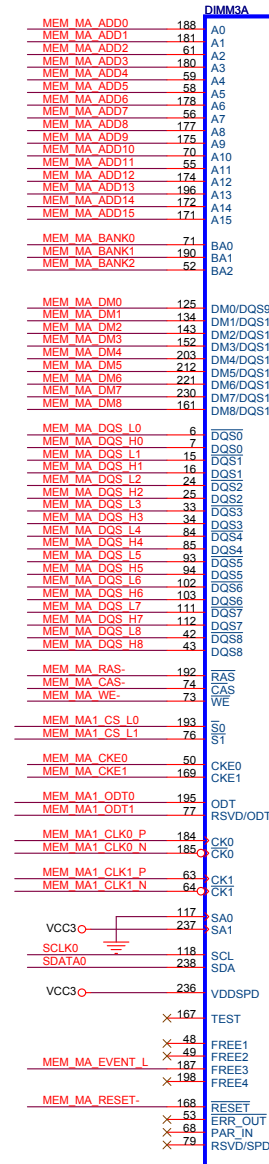
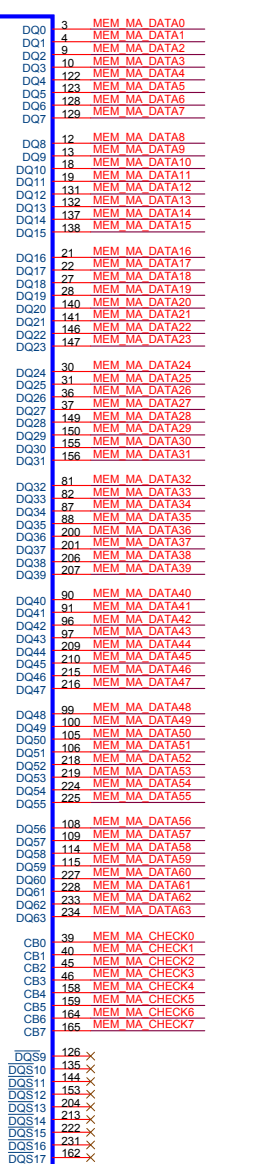


SMBus Addressing

SMBus 0	
Device	8-bit Address (hex)
DIMMA0	A0
DIMMB0	A2
DIMMA1	A4
DIMMB1	A6

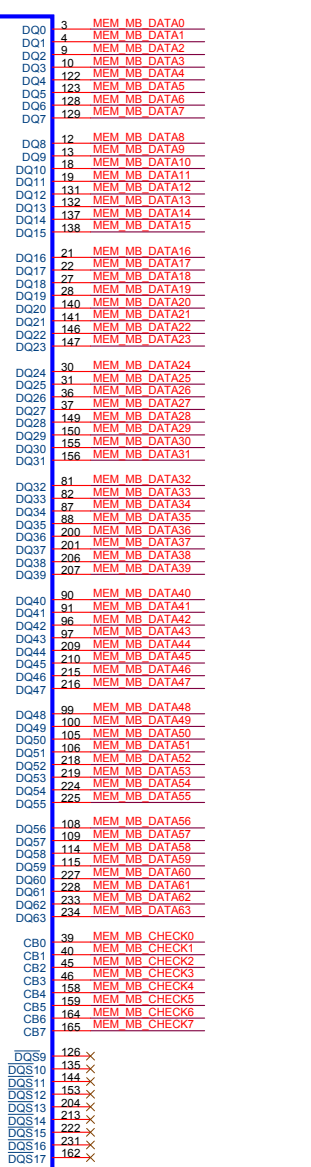
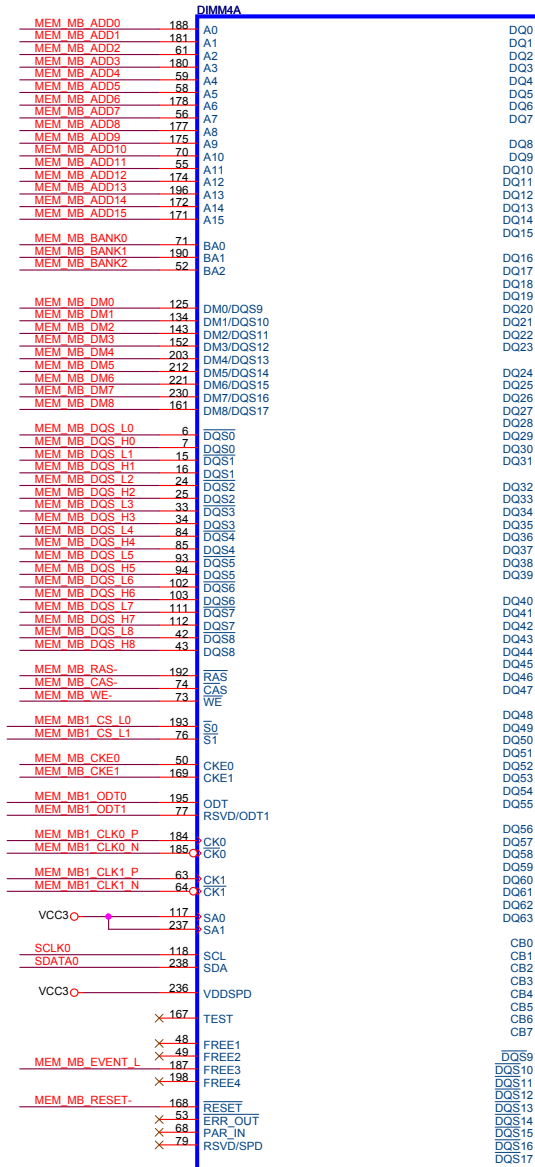
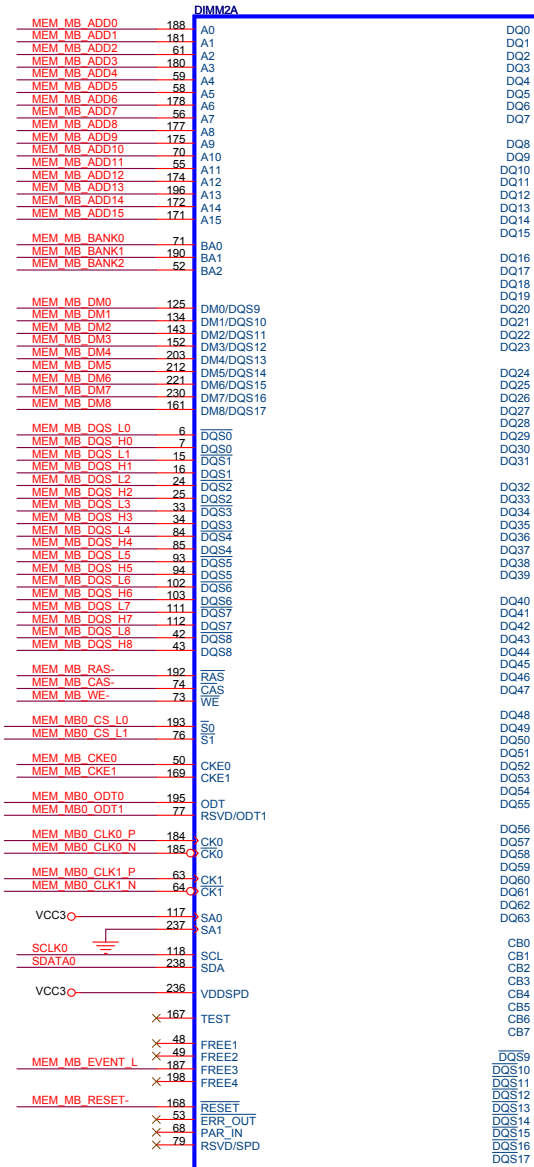
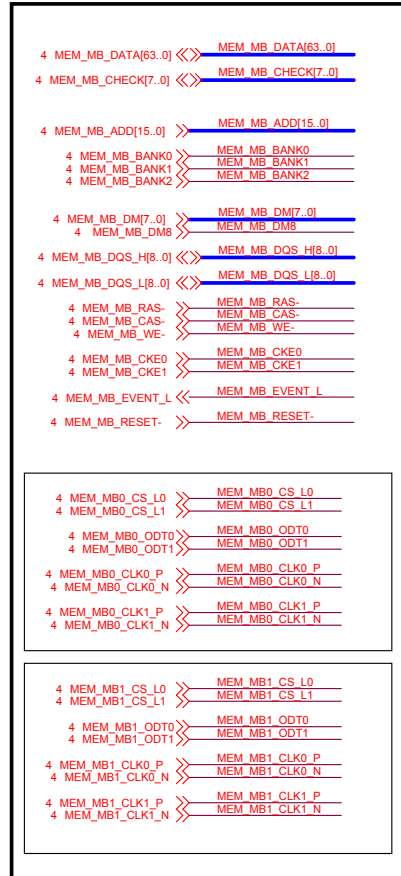
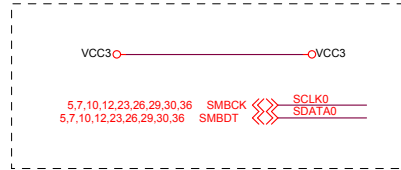


DDR3-240-OR

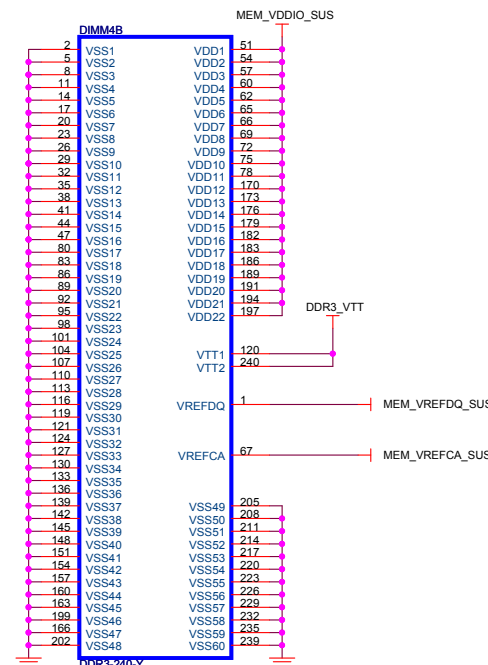
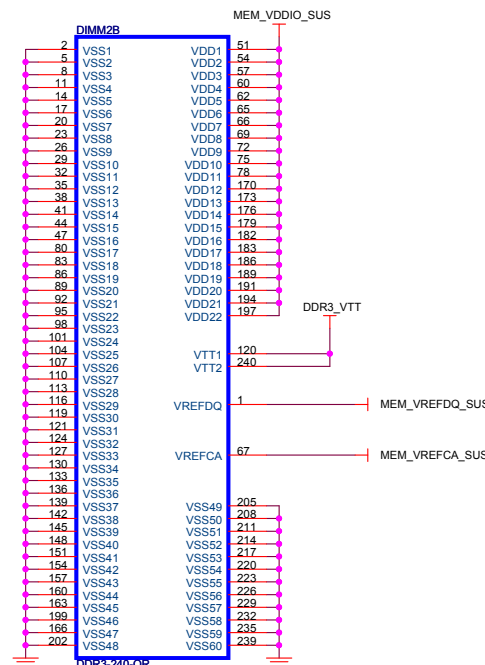
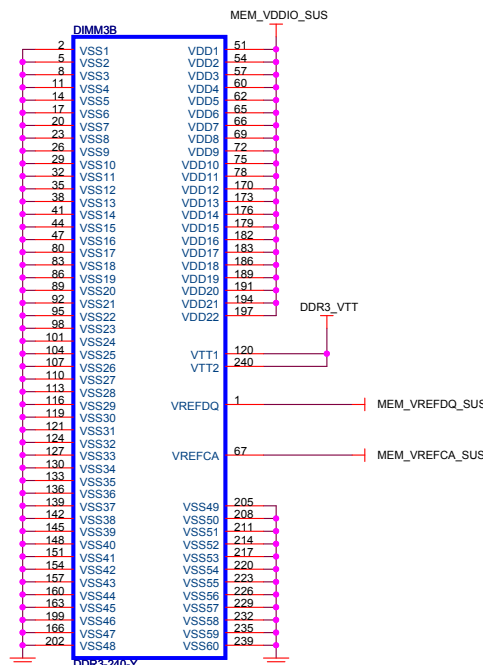
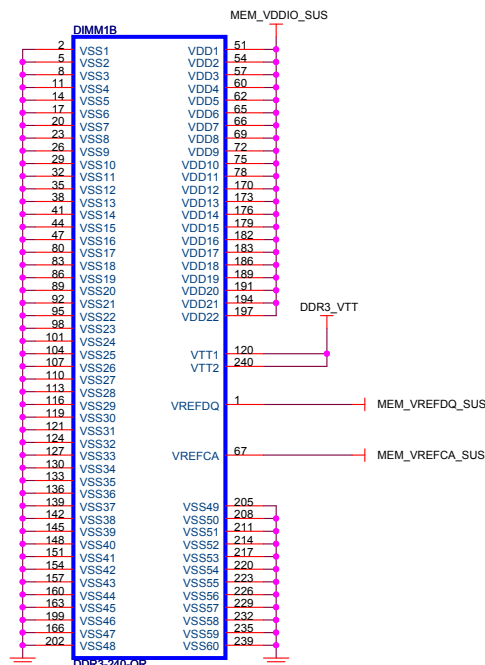
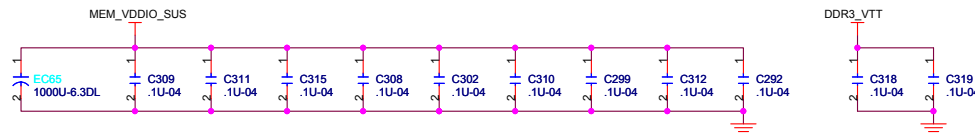
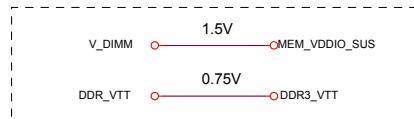


DDR3-240-Y

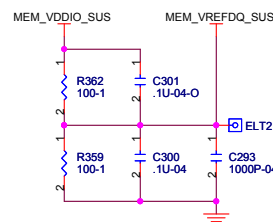
B Chanel



DE-COUPLING CAP FOR DIMMs

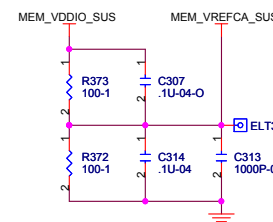


MEM_VREFDQ_SUS



Layout: Place within 500 mils of the DIMMB1(4) socket.

MEM_VREFCA_SUS



Layout: Place within 500 mils of the DIMMB1(4) socket.



- 1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE TO CLK. GEN. AS POSSIBLE
- 2- ROUTE ALL SRCCLKTx AND SRCCLKx AS DIFFERENT PAIR RULE
- 3- PUT DECOUPLING CAPS CLOSE TO CLK. GEN. POWER PIN

Place R164 less than 100 mils away from Clk. Gen. and route CPU clock as 100ohm impedance with differential pair

NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780	
HT_REFCLKP	66M SE(SE)	100M DIFF	100M DIFF	
HT_REFCLKN	NC	100M DIFF	100M DIFF	
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)	100M DIFF
REFCLK_N	NC	NC	vref	100M DIFF
GFX_REFCLK	100M DIFF	100M DIFF	100M DIFF(IN/OUT)*	
GPP_REFCLK	NC	100M DIFF	100M DIFF(OUT)	
GPSPB_REFCLK	100M DIFF	100M DIFF	100M DIFF	

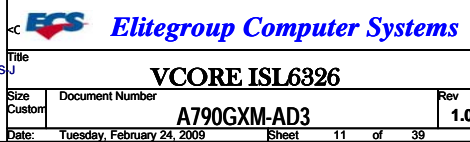
* RS780 can be used as clock buffer to output two PCIe reference clocks
By default, chip will configured as input mode, BIOS can program it to output mode.

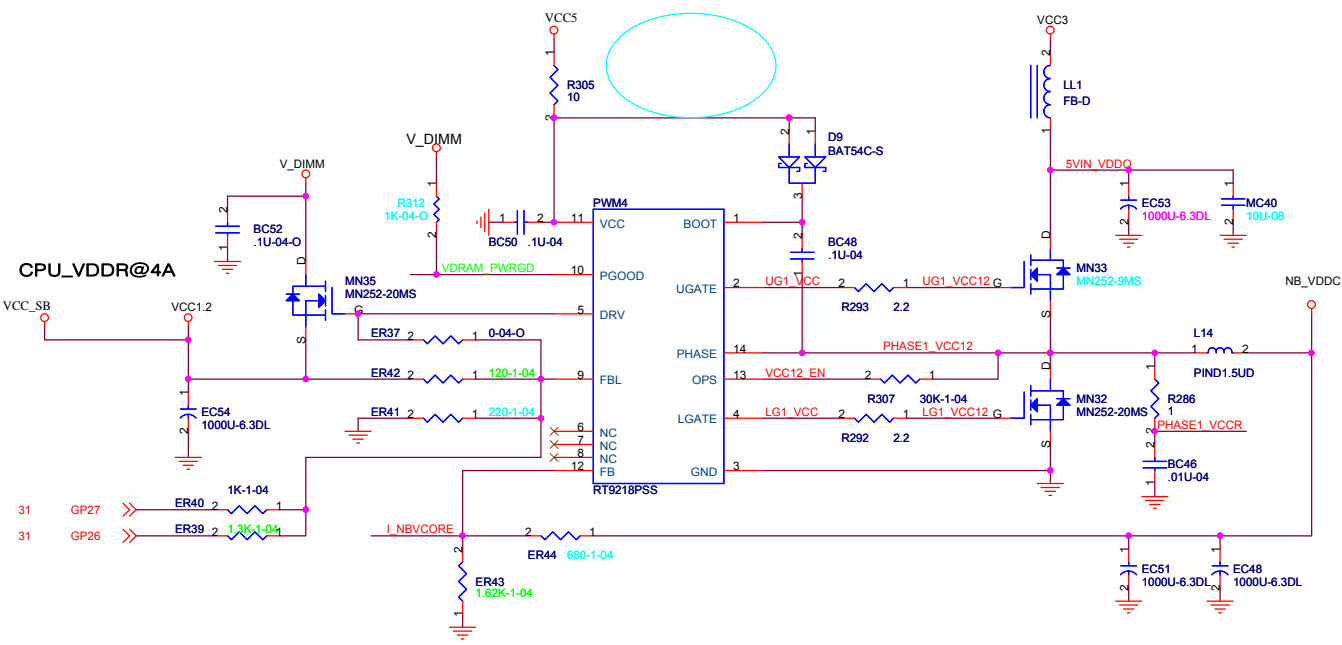
REF0/SEL_HTT66	HTT CLOCK
0	100.00 DIFFERENTIAL
1	66.66 SINGLE END

REF1/SEL_SATA	SRC6/SATA
0	100.00 DIFFERENTIAL SPREADING SRC CLOCK
1	100.00 NON-SPREADING DIFFERENTIAL SATA CLOCK

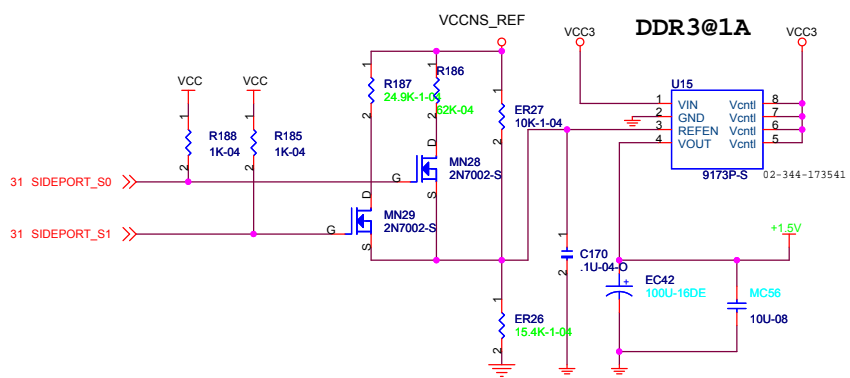
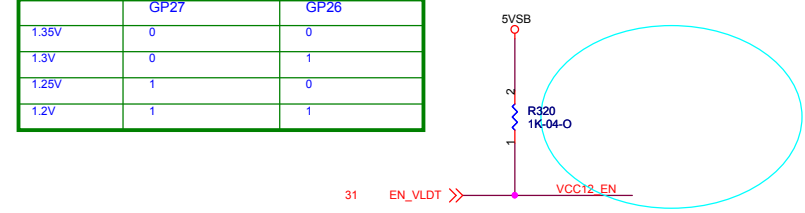
	OSC_14M_SB
SB750-A12	R161 Open
SB750-A14	R161 Add & New BIOS

	OSC_14M_NB
RS740	3.3V 33R serial
RX780	1.8V 75R/100R
RS780 (Single-ended)	1.1V 150R(R165) /75R(R162)

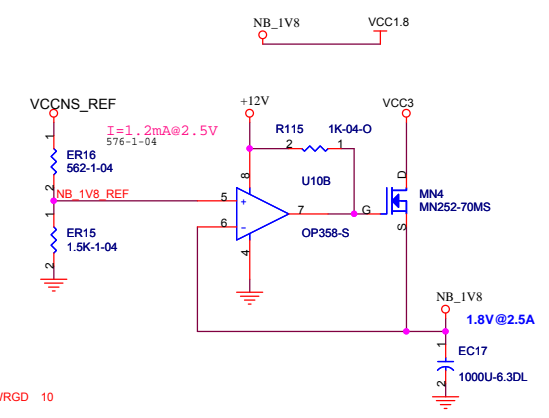
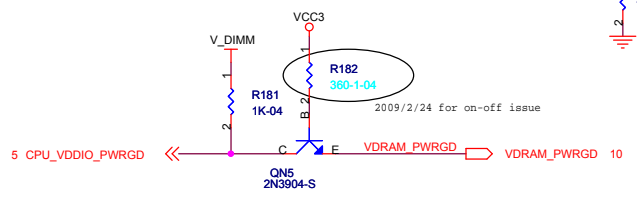
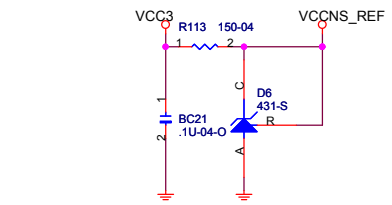
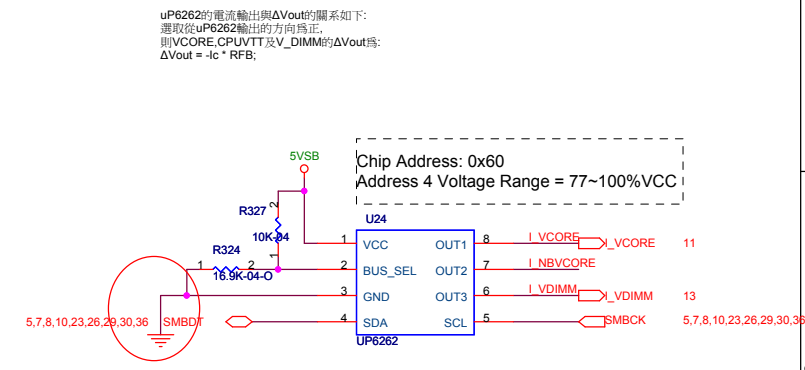


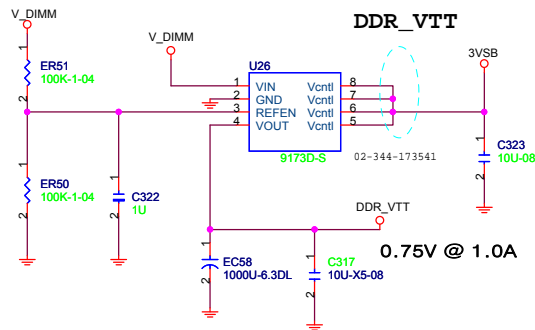
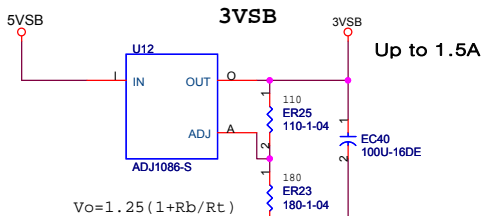
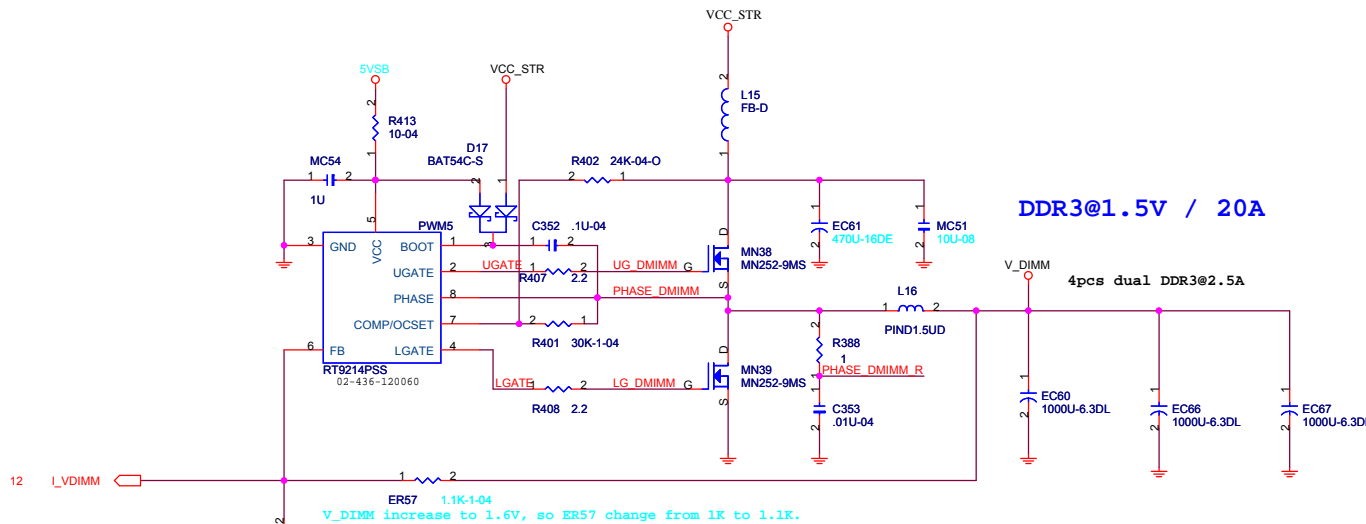


	GP27	GP26
1.35V	0	0
1.3V	0	1
1.25V	1	0
1.2V	1	1

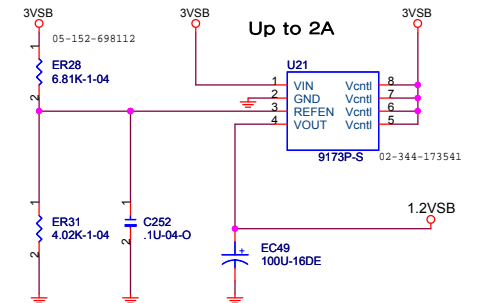


	SIDEPORT_S1	SIDEPORT_S0
1.512	0	0
1.602V	0	1
1.705V	1	0
1.763V	1	1

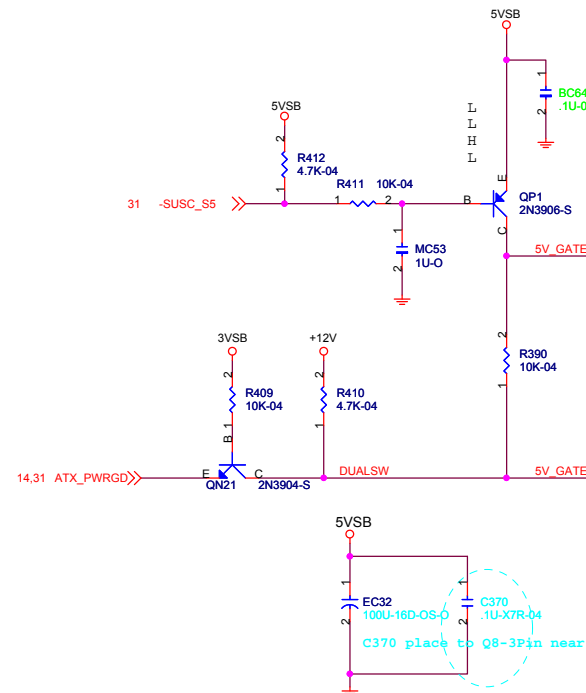
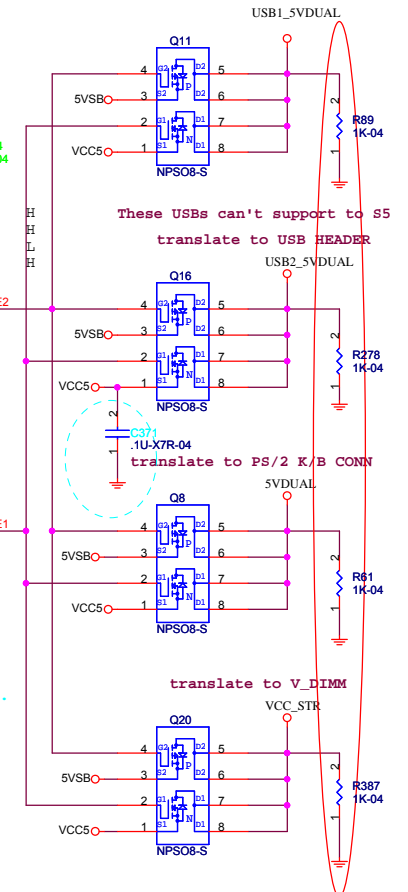




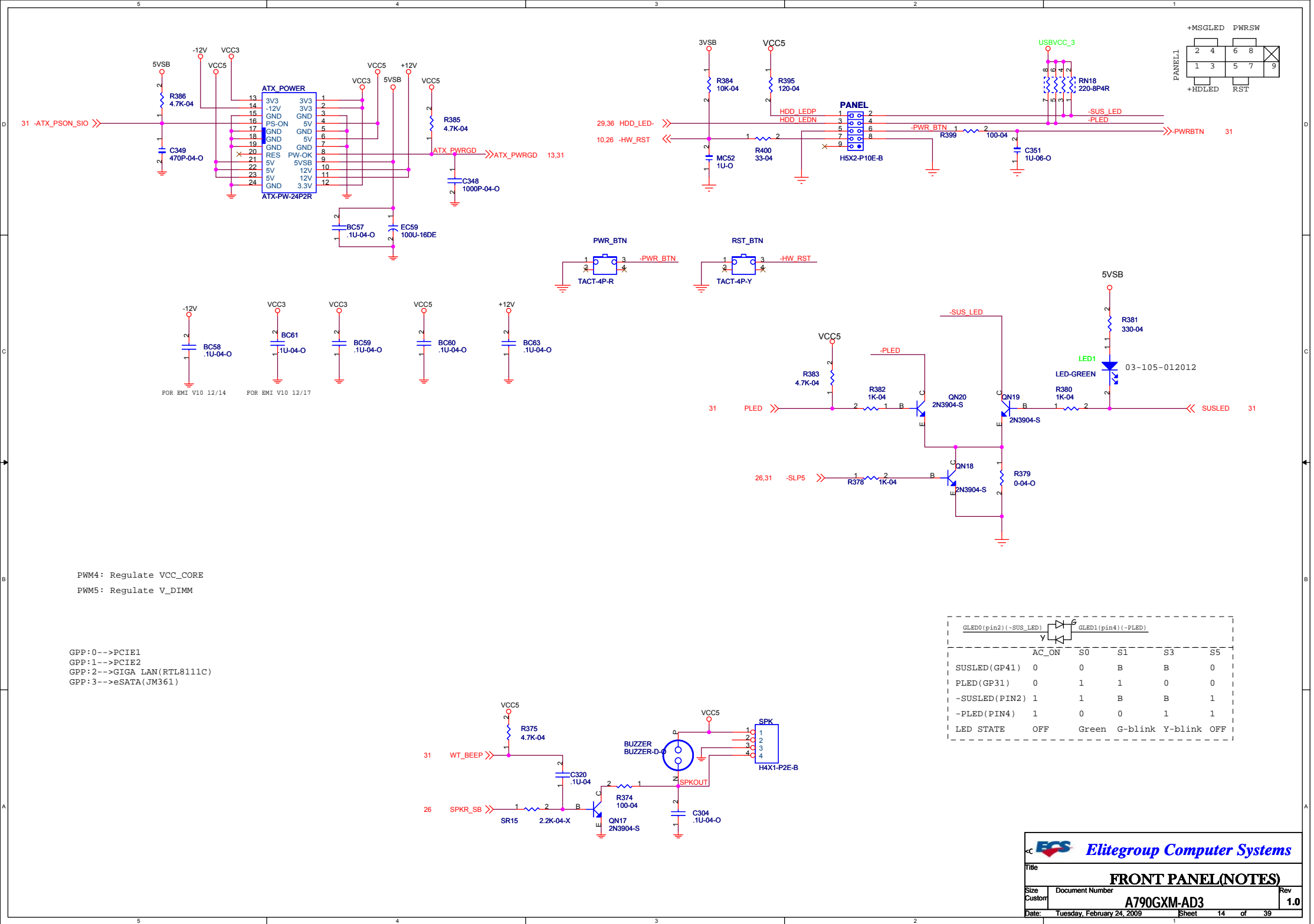
1.2VSB

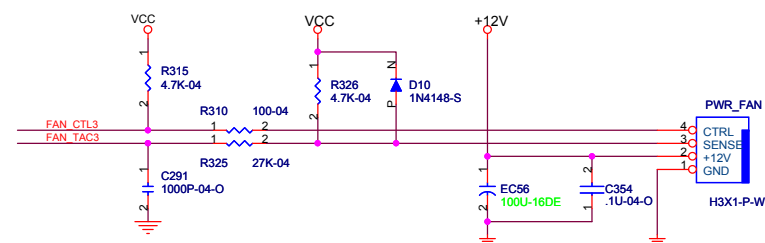
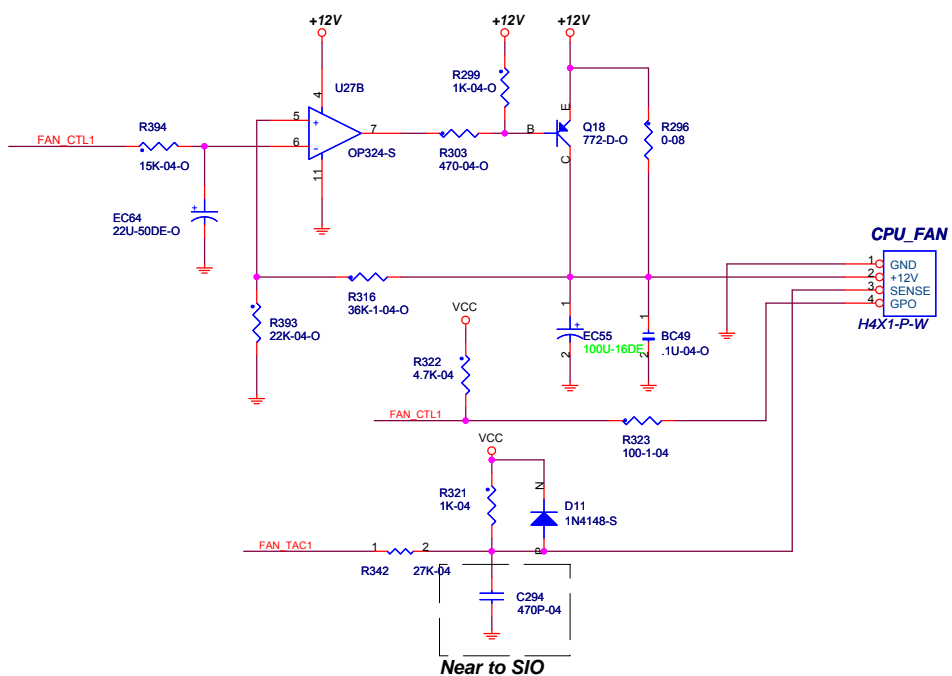
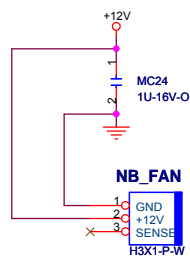


translate to Rear I/O Connector



	S5	enter	S0	enter	S3	exit	S3	enter	S5	S5
-SUSC_S5	0	0	1	1	1	0	0	0	0	0
ATX_PWRGD	0	1	1	0	1	1	0	0	0	0
QP1 pinC	5VSB=0	5VSB=0	12V	0	12V	5VSB=1	5VSB=1	0	0	0
DUALSW	0	12V	12V	0	12V	12V	0	0	0	0
VCCSTR/Out	X	VCC5	VCC5	5VSB=1	VCC5	VCC5	0	0	0	0
VDIMM	X	V	V	V	V	V	0	0	0	0

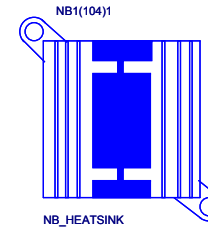


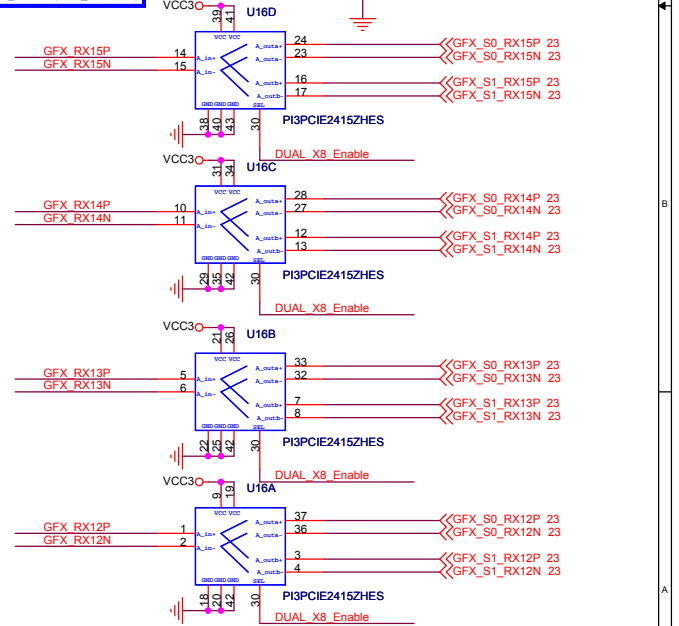
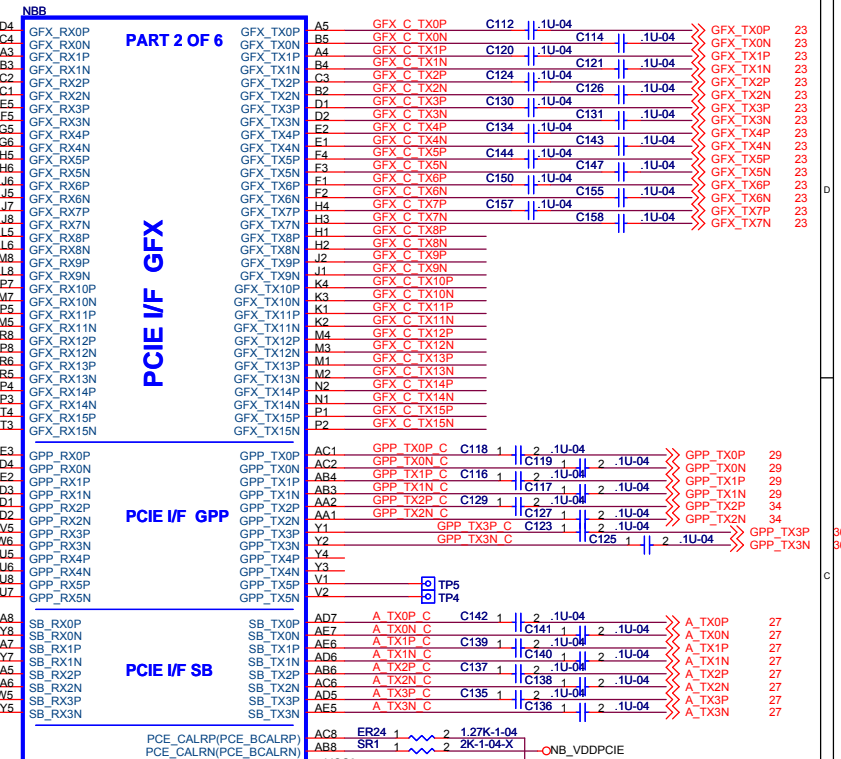
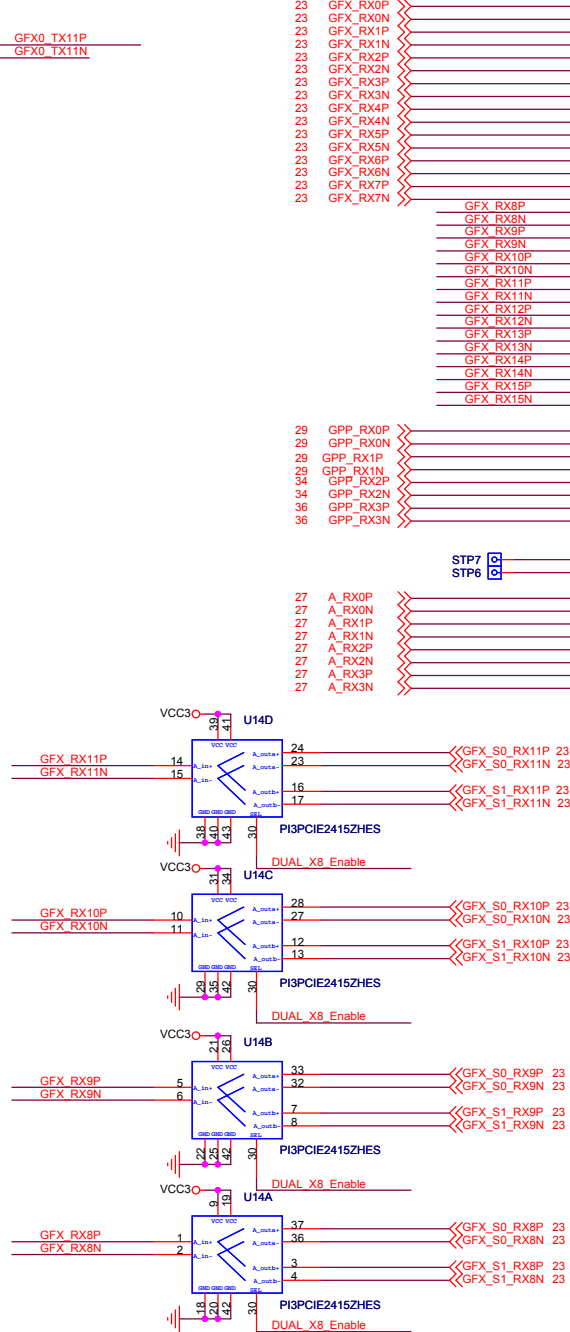
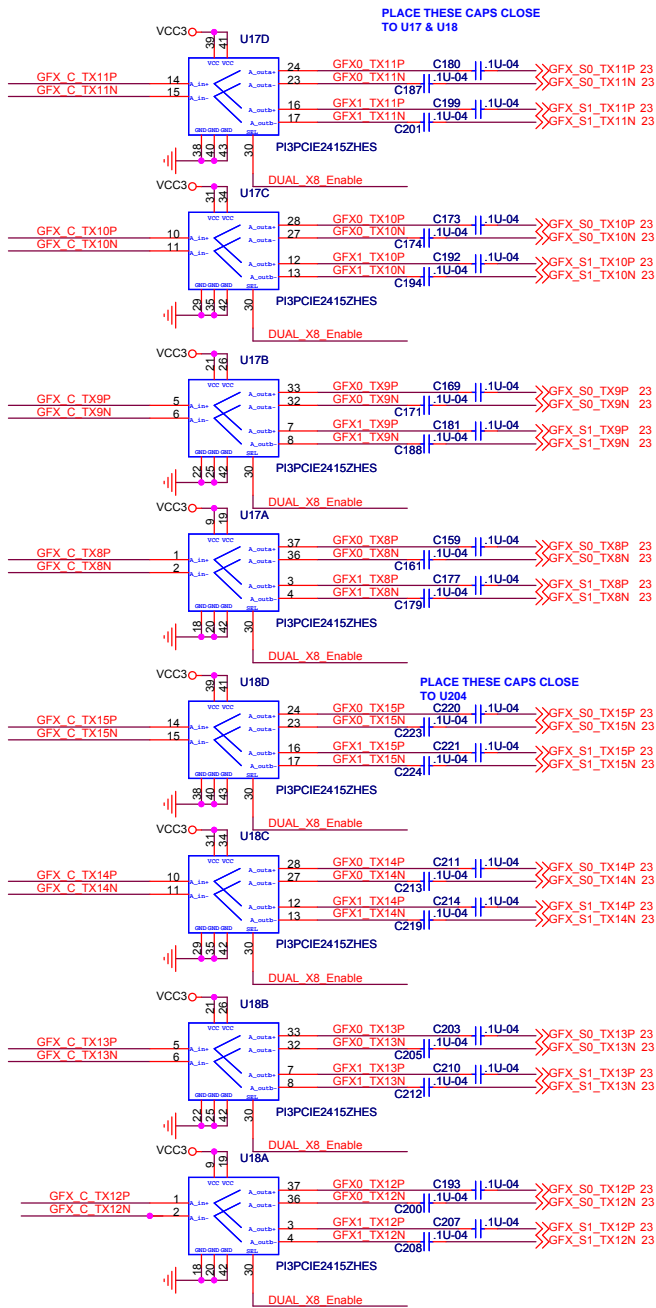




RX780/RS740/RS780 difference table (HT LINK)

SIGNALS	RS740	RX780	RS780
HT_RXCALP	49.9R (GND)	1.21K	301R
HT_RXCALN	49.9R (VDDHT)		
HT_TXCALP	100R *	1.21K	301R
HT_TXCALN			





RS780 GFX Slot Routing table

GFX_MODE_SELECT	GFX SLOTS MODE
0	X16 LANES MODE (DEFAULT)
1	TWO X8 LANES MODE

RS780 GPP Routing table

	RS780
PCIE1 CONNECTOR	GPP:[0]
PCIE2 CONNECTOR	GPP:[1]
GIGA LAN/RTL8111C)	GPP:[2]
eSATA/JM361	GPP:[3]

DUAL X8_Enable <<<GFX_MODE_SEL 26

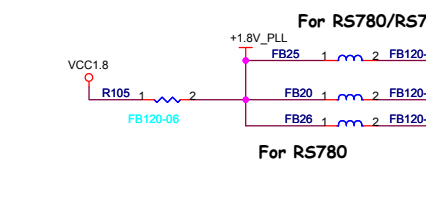
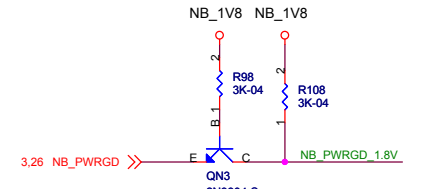
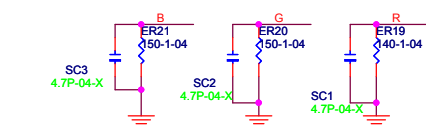
Elitegroup Computer Systems

Title: **RS790GX PCIE**

Size: **A790GXM-AD3**

Document Number: **Rev 1.0**

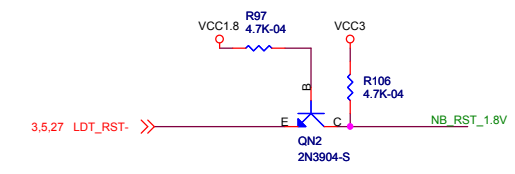
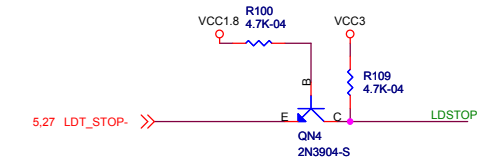
Date: Tuesday, February 24, 2009 Sheet 17 of 39



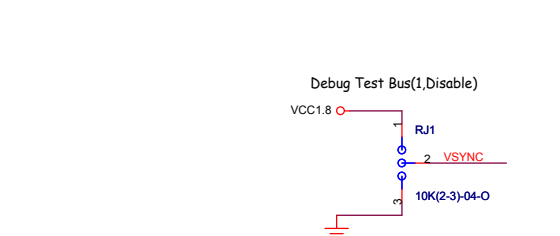
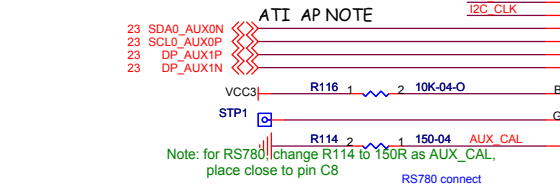
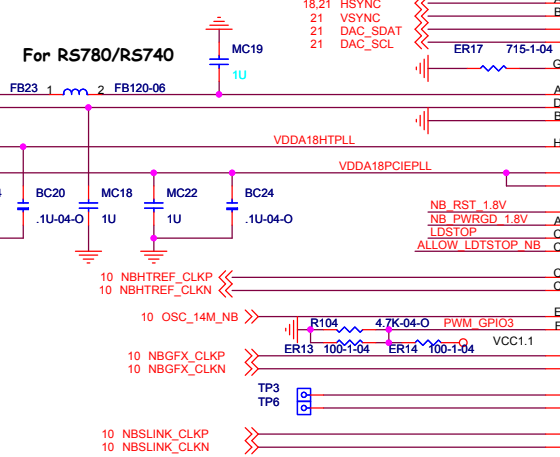
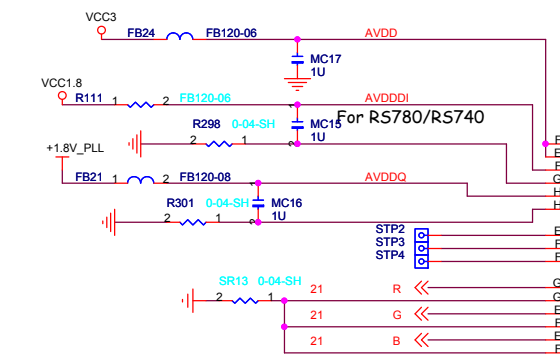
RX740/RS740/RS780 difference table

	RS740	RX780	RS780/D
NB_PWRGD IN	3.3V IN	1.8V IN	1.8V IN
ALLOW_LDTSTOP OUT(default)/IN	OC	OC	OC/3.3V IN
LDT_STOP# IN(default)/OUT	3.3V IN	1.8V IN	3.3V IN/OC
SYSTEMRESETb IN	3.3V IN	1.8V IN	3.3V IN

*, CLMC mode: NB send LDT_STOP#, ALLOW_LDTSTOP will become input



27 ALLOW_LDTSTOP NB output is OD pin



RS740/RX780/RS780/D: STRAP_DEBUG_BUS_GPIO_ENABLE

Enables the Test Debug Bus using GPIO and/or memory IO

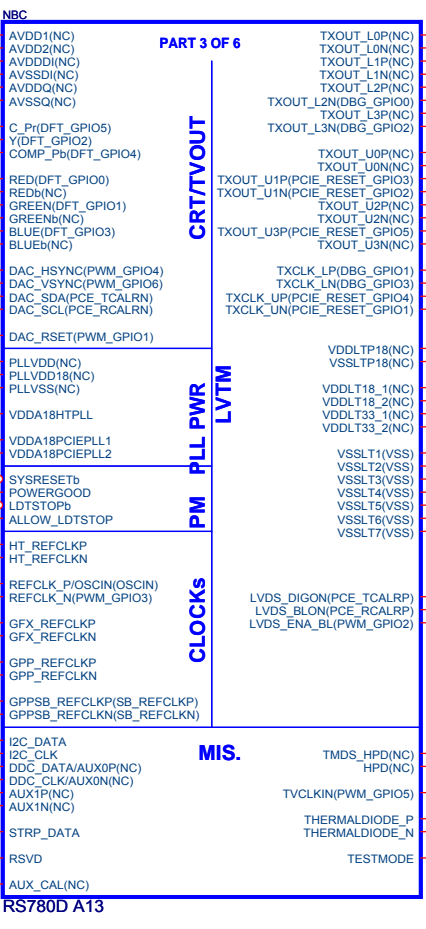
1 : Disable (RS740); Enable (RX780/RS780)

0 : Enable (RS740); Disable(RX780/RS780)

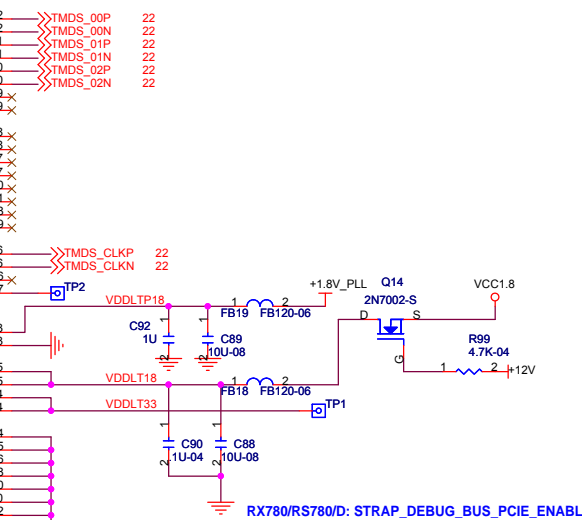
RS740: pin DFT_GPIO5

RX780: pin DFT_GPIO5

RS780: pin VSYNC



RS780D A13



RX780/RS780/D: STRAP_DEBUG_BUS_PCIE_ENABLE

Enables Test debug bus using PCIe bus

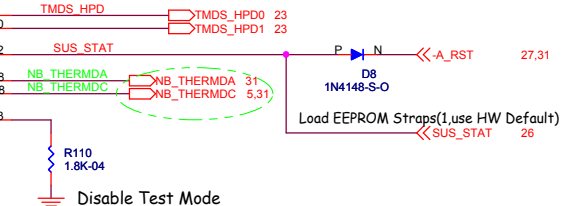
1. Disable (can be enabled thru nbcfg register)

0 : Enable

RX780: pin DFT_GPIO0

RS780: configurable thru register setting only

RS740: Not supported



RS740/RX780/RS780/D: LOAD_EEPROM_STRAPS

Selects Loading of STRAPS from EPROM

1 : Bypass the loading of EEPROM straps and use Hardware Default Values

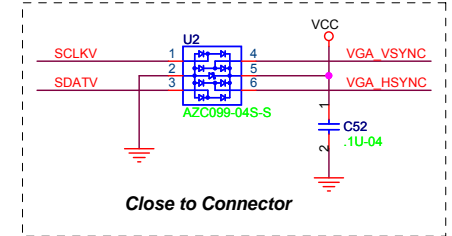
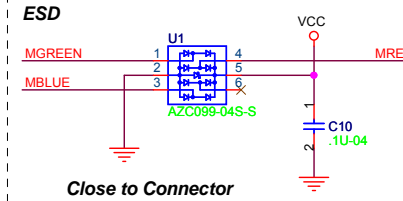
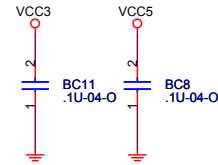
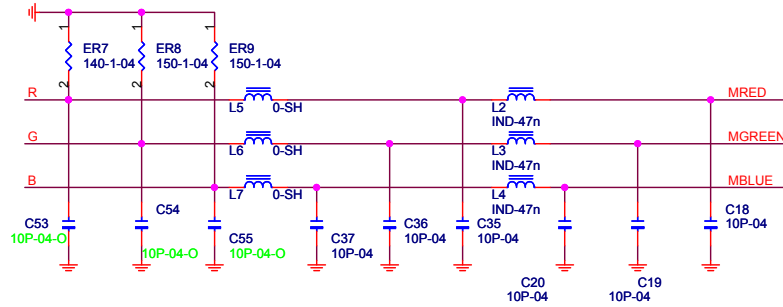
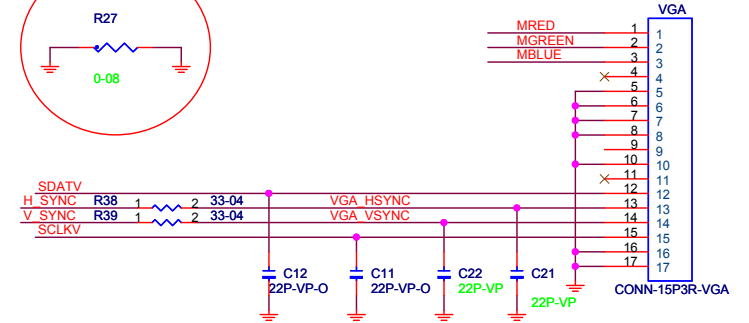
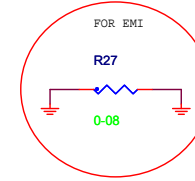
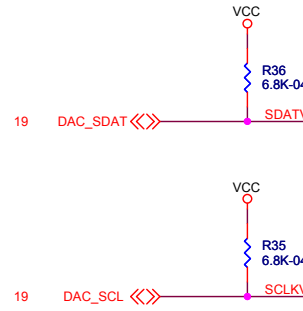
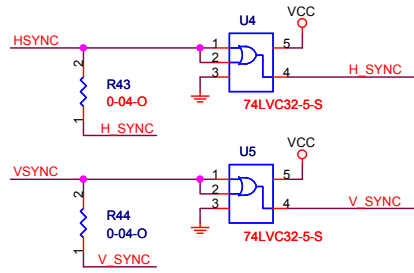
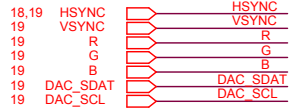
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

RS740: pin DFT_GPIO1

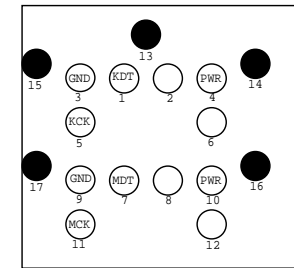
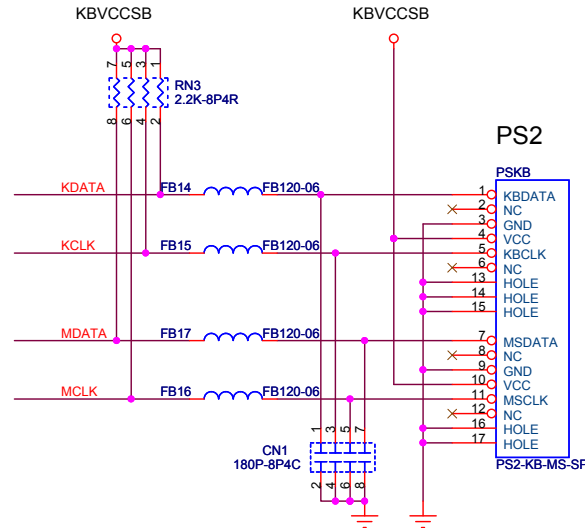
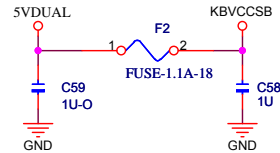
RX780: pin DFT_GPIO1

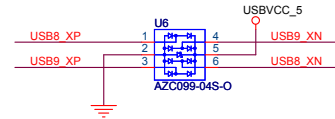
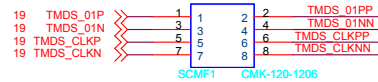
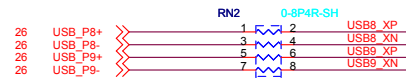
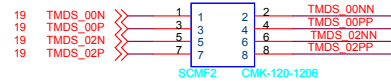
RS780: pin SUS_STAT#

External Connection

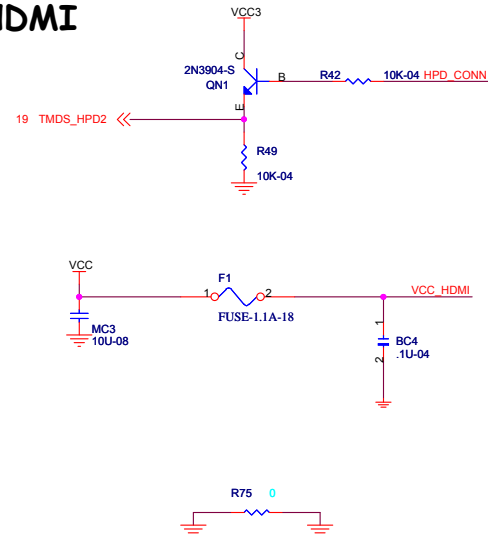
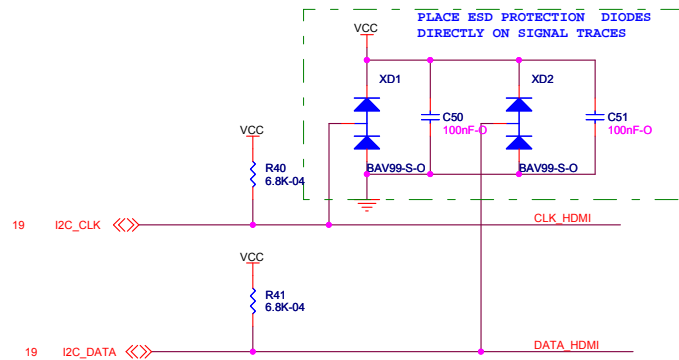


KEYBOARD & MOUSE

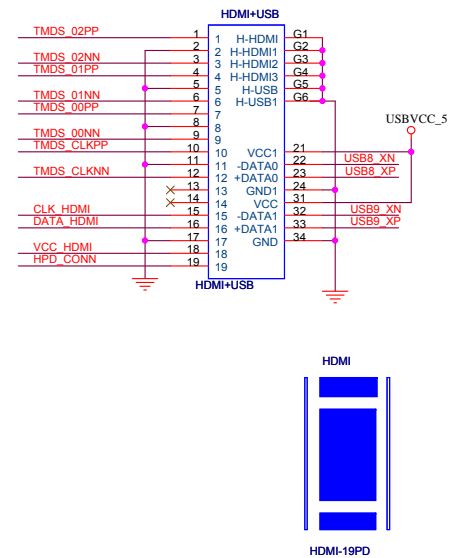


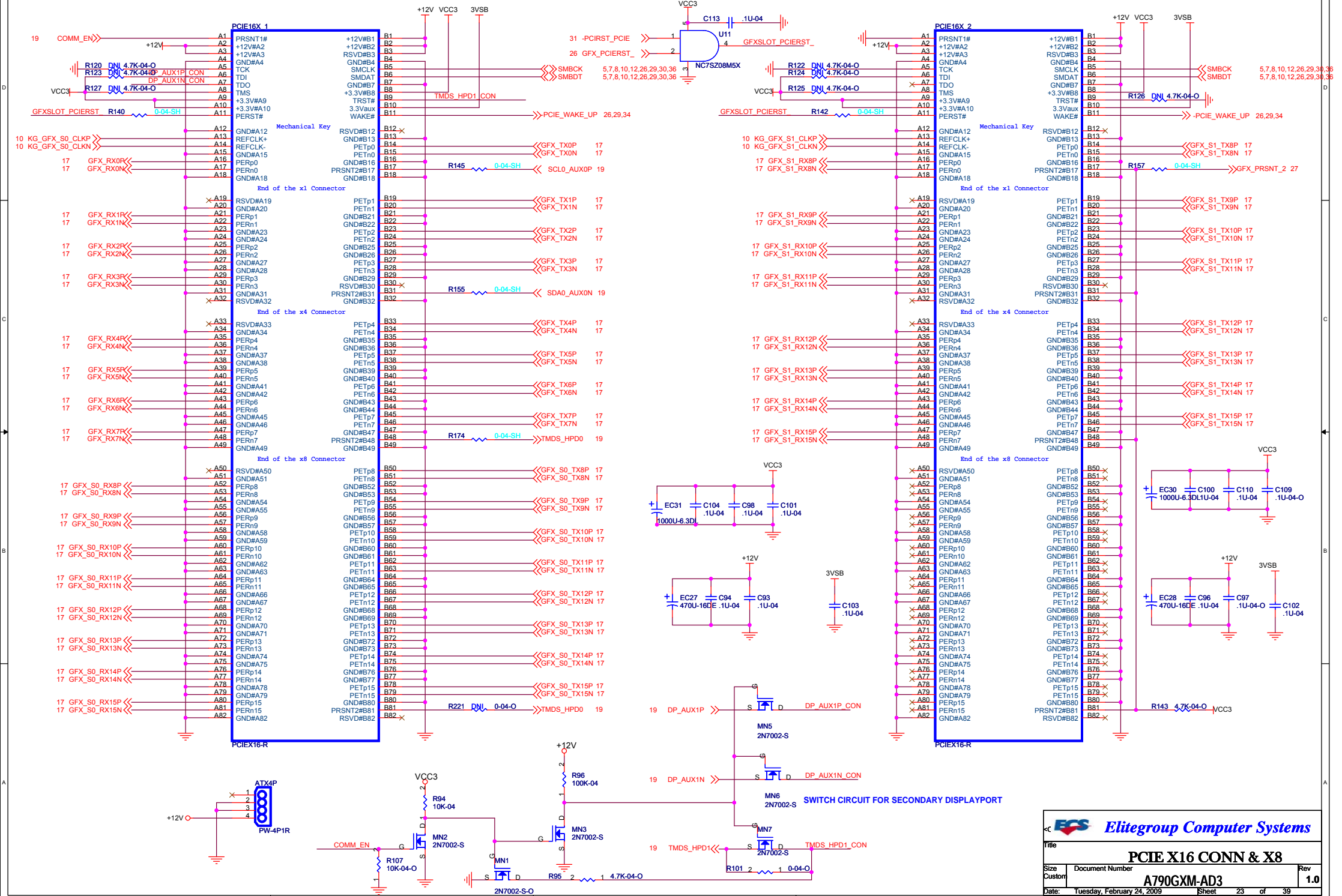


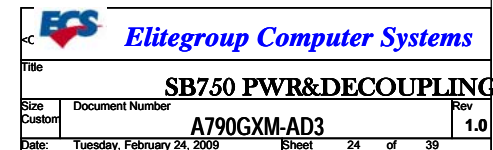
HDMI



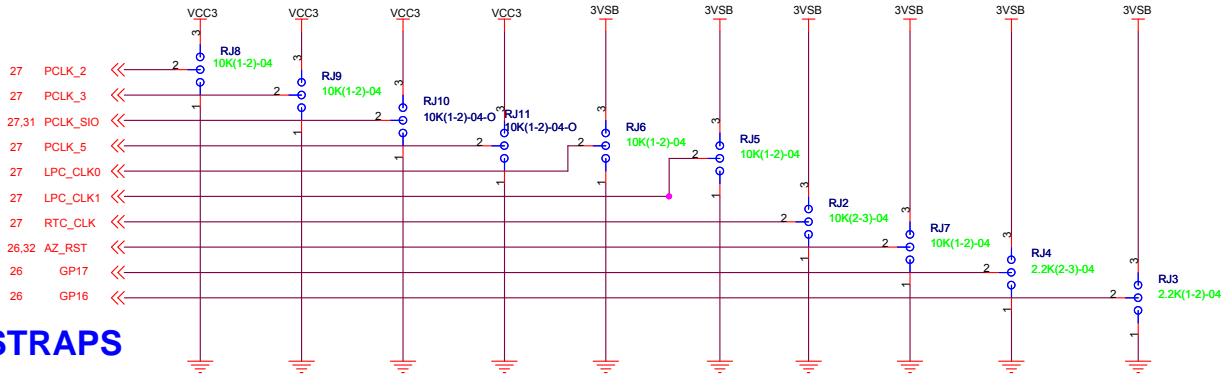
USB8,9







NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK



OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

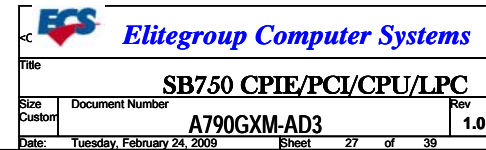
REQUIRED STRAPS

	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	AZ_RST#	GP17	GP16
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	IMC ENABLED	CLKGEN ENABLED	INTERNAL RTC DEFAULT	EC ENABLED	ROM TYPE: H, H = Reserved H, L = SPI ROM DEFAULT	
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			IMC DISABLED DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT	L, H = LPC ROM L, L = FWH ROM	

DEBUG STRAPS SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]

Del PCIE Debug EEPROM Strap

Del Debug straps 070423

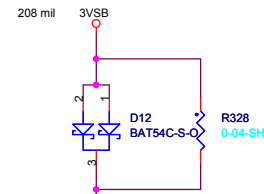
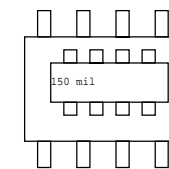




Note: Do we still keep mobile SATA connector?
Is there any side affect to test RAID mode?

PLACE SATA AC COUPLING
CAPS CLOSE TO SB700

SO8 MN and MW co-layout layout draw



SB700
Part 2 of 5

SERIAL ATA

ATA 66/100/133

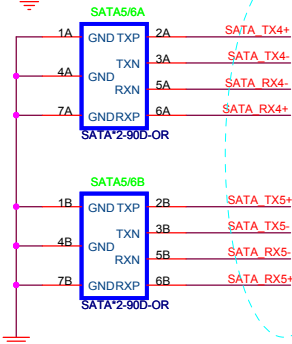
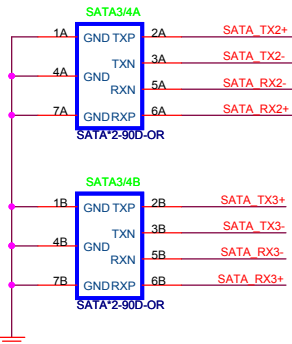
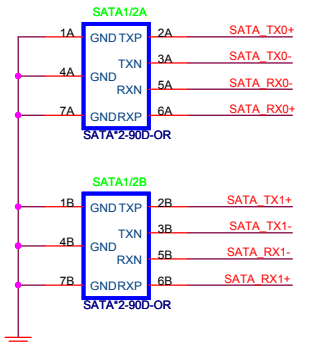
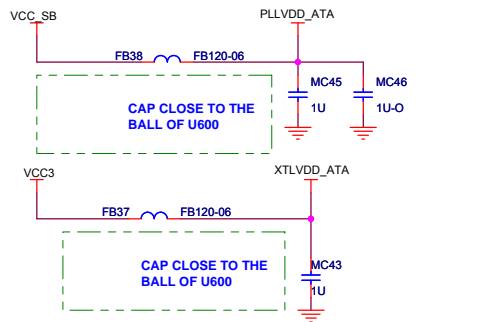
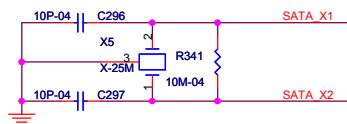
SPI ROM

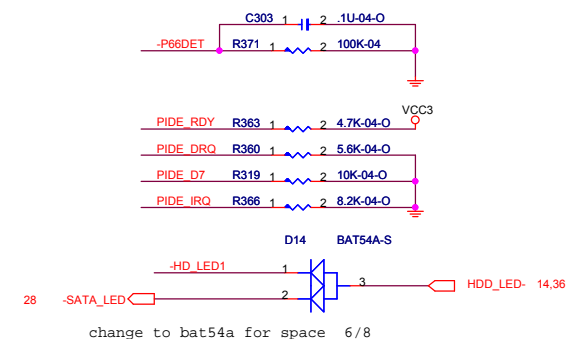
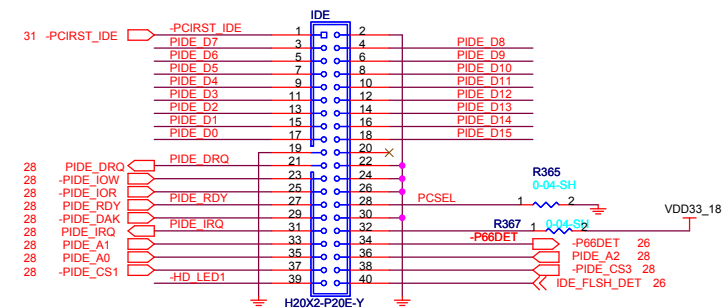
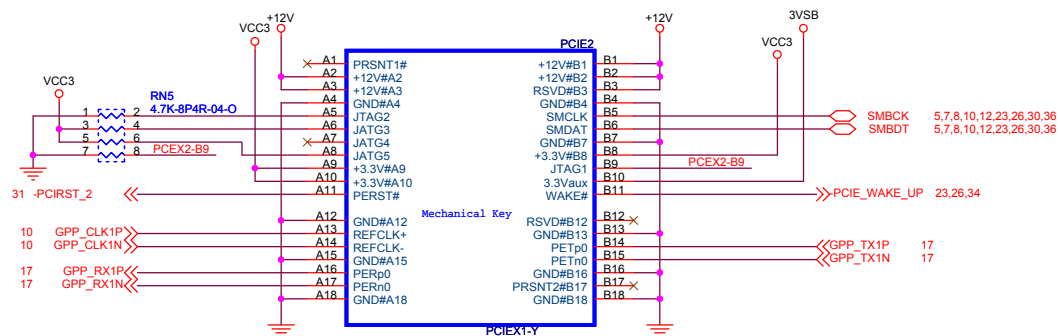
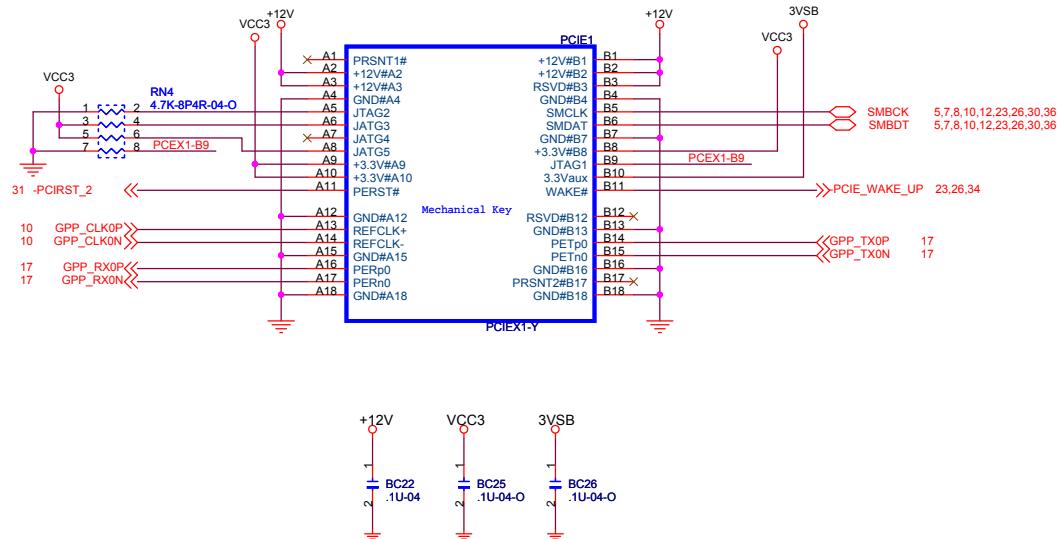
HW MONITOR

SATA PWR

PLACE SATA_CAL
RES VERY CLOSE
TO BALL OF SB700

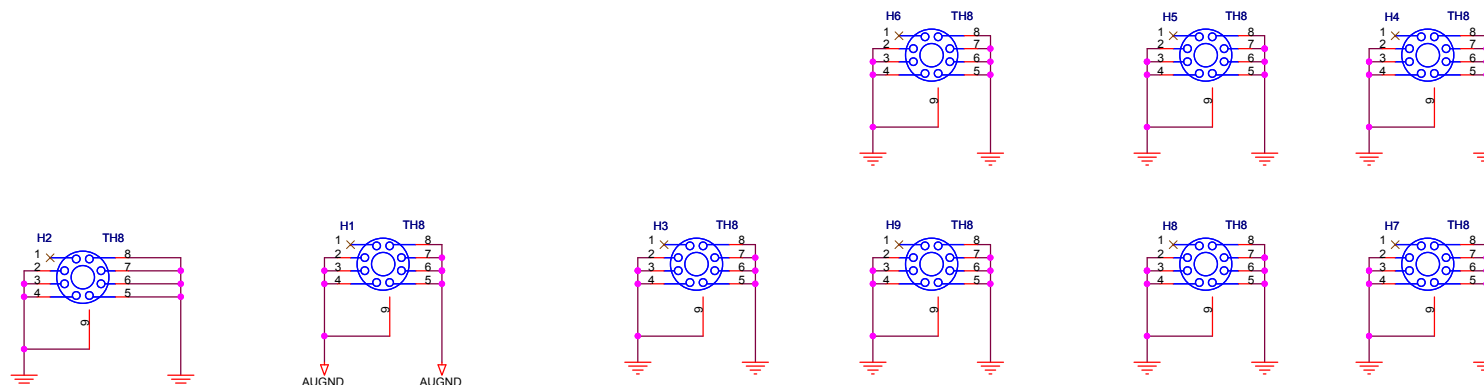
NOTE:
SR2 IS 1K 1% FOR 25MHz
XTAL, 4.99K 1% FOR 100MHz
INTERNAL CLOCK



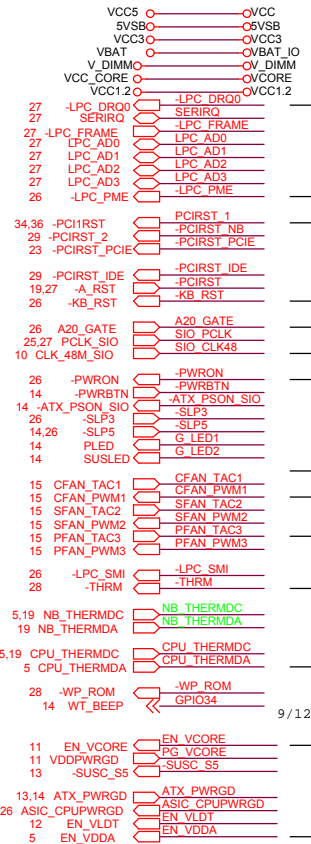


28 PIDE_D[15:0]

change to bat54a for space 6/8

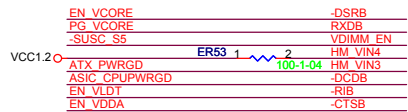


External Connection

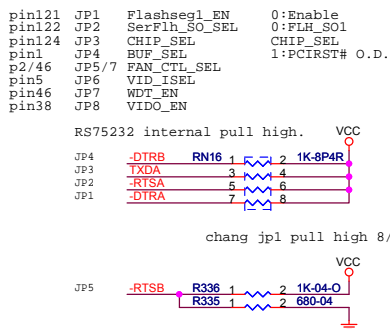


If you found anything wrong with this circuit, please contact with Jack Hu (Ext:622)

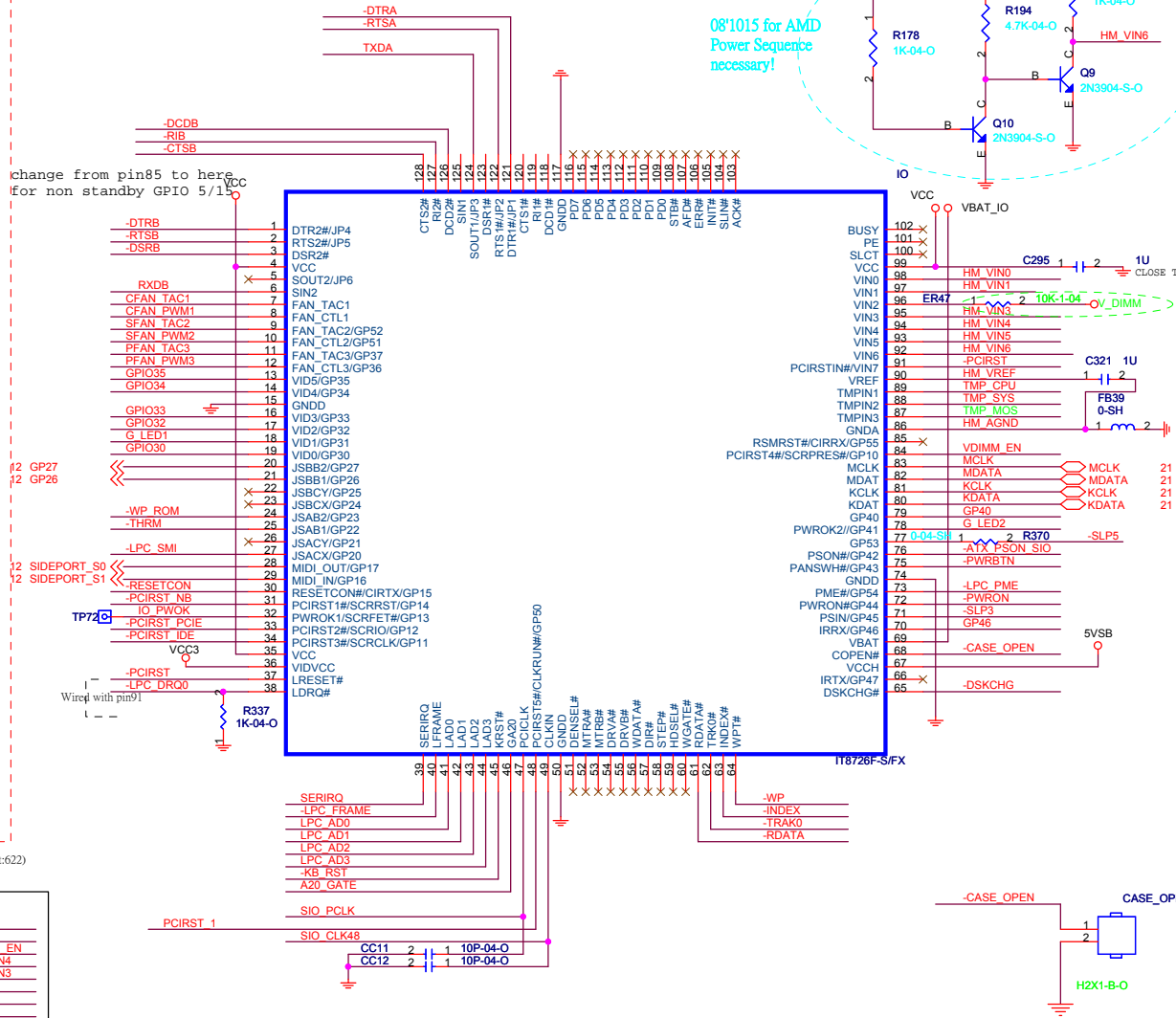
For COM2 co-lay



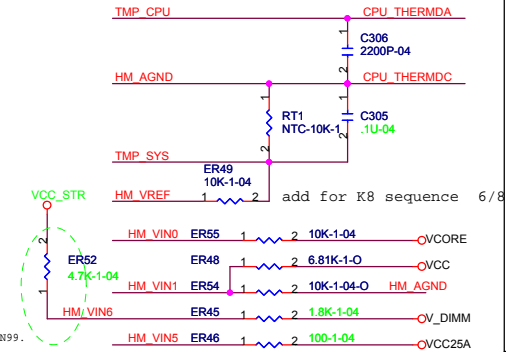
HW STRAPPING



del 5VSB and NBPWM control GPIO 6/8



Thermal Monitor



* HM_VIN0 for VCORE

* HM_VIN1 for VCC

HM_VIN5 for 2.5V

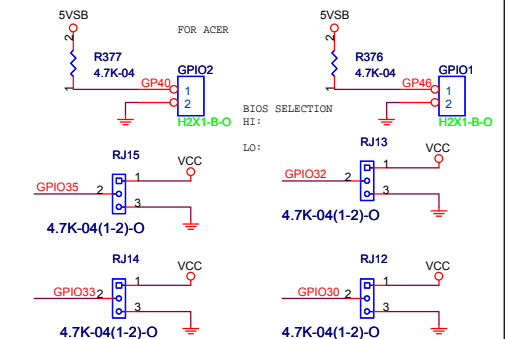
HM_VIN3 for ATX PWRGD

HM_VIN2 for VCC3

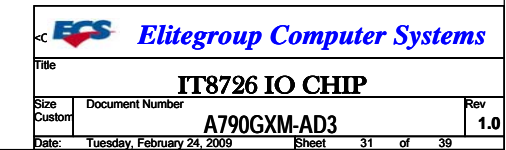
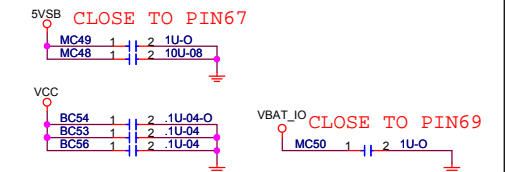
HM_VIN4 for VLDT 1.2V I/P

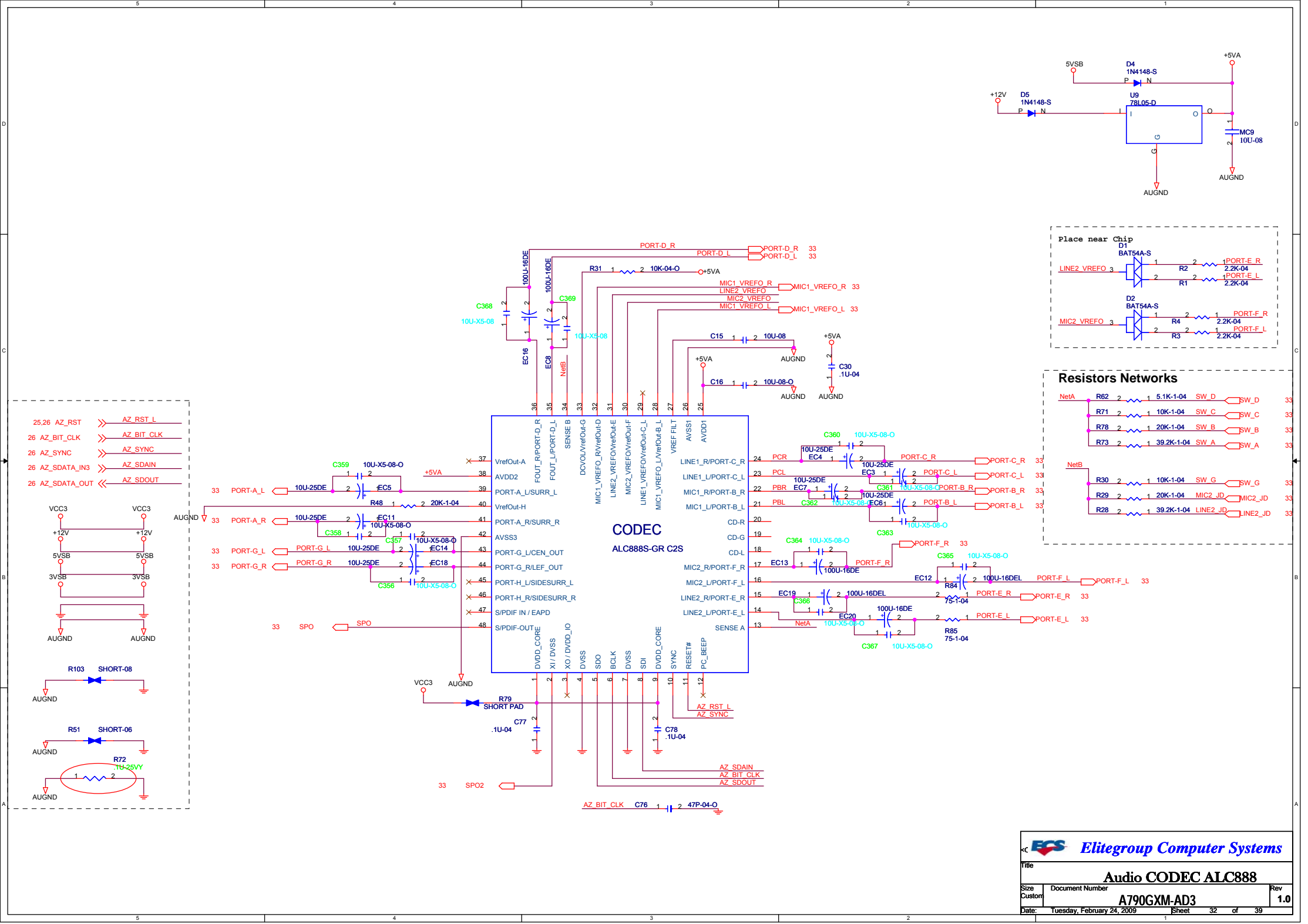


BIOS SELECTION



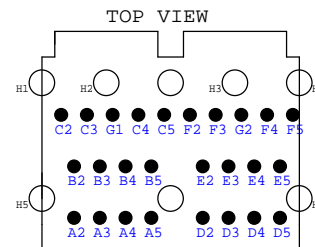
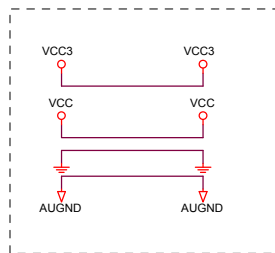
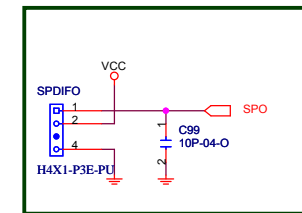
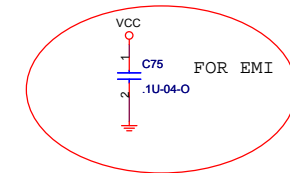
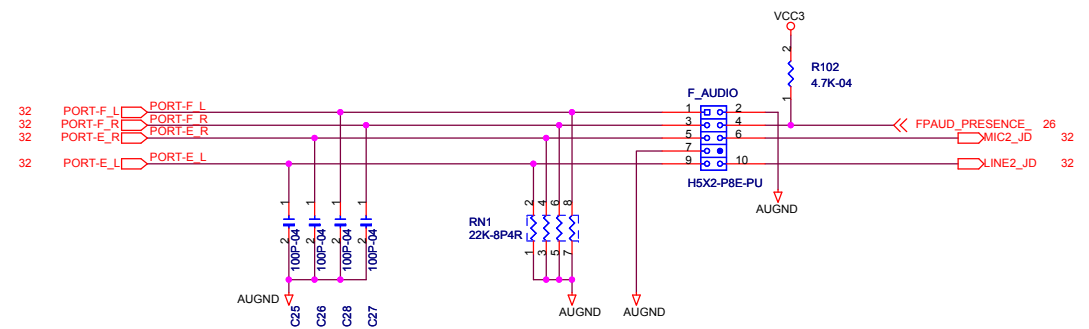
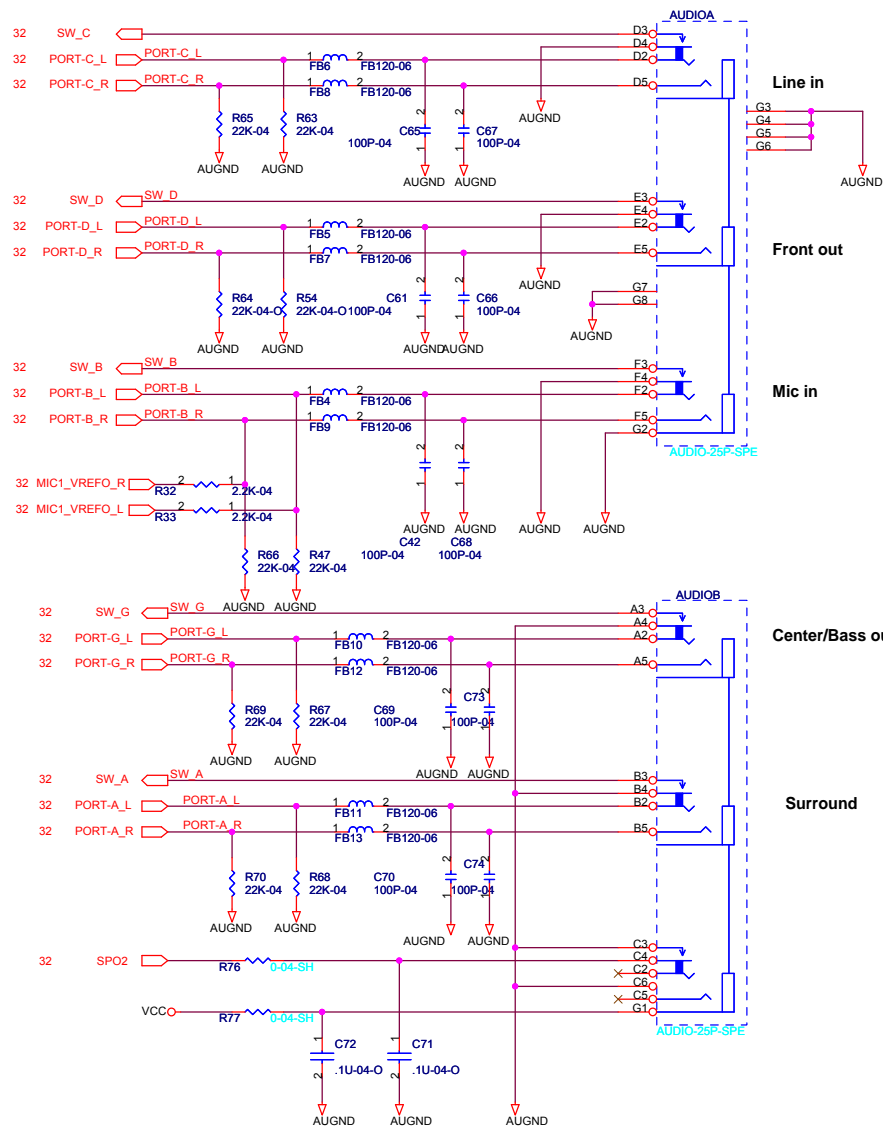
	BYPASS CAP
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Date: Tuesday, February 24, 2009

Sheet 32 of 39



USB VCC1 3VSB VCC3 AUGND2

USB B- AUGND2

23, 26, 29, 32 PCIE_WAKE_UP PCIE LAN RST

31, 36 PCIE LAN RST

17 GPP_TX2P LAN_HSP

10 GB_CLKP CK PE LANP

10 GB_CLKN CK PE LANN

17 GPP_RX2P LAN_HSP

17 GPP_RX2N LAN_HSP

26 USB_P0+ USB C+

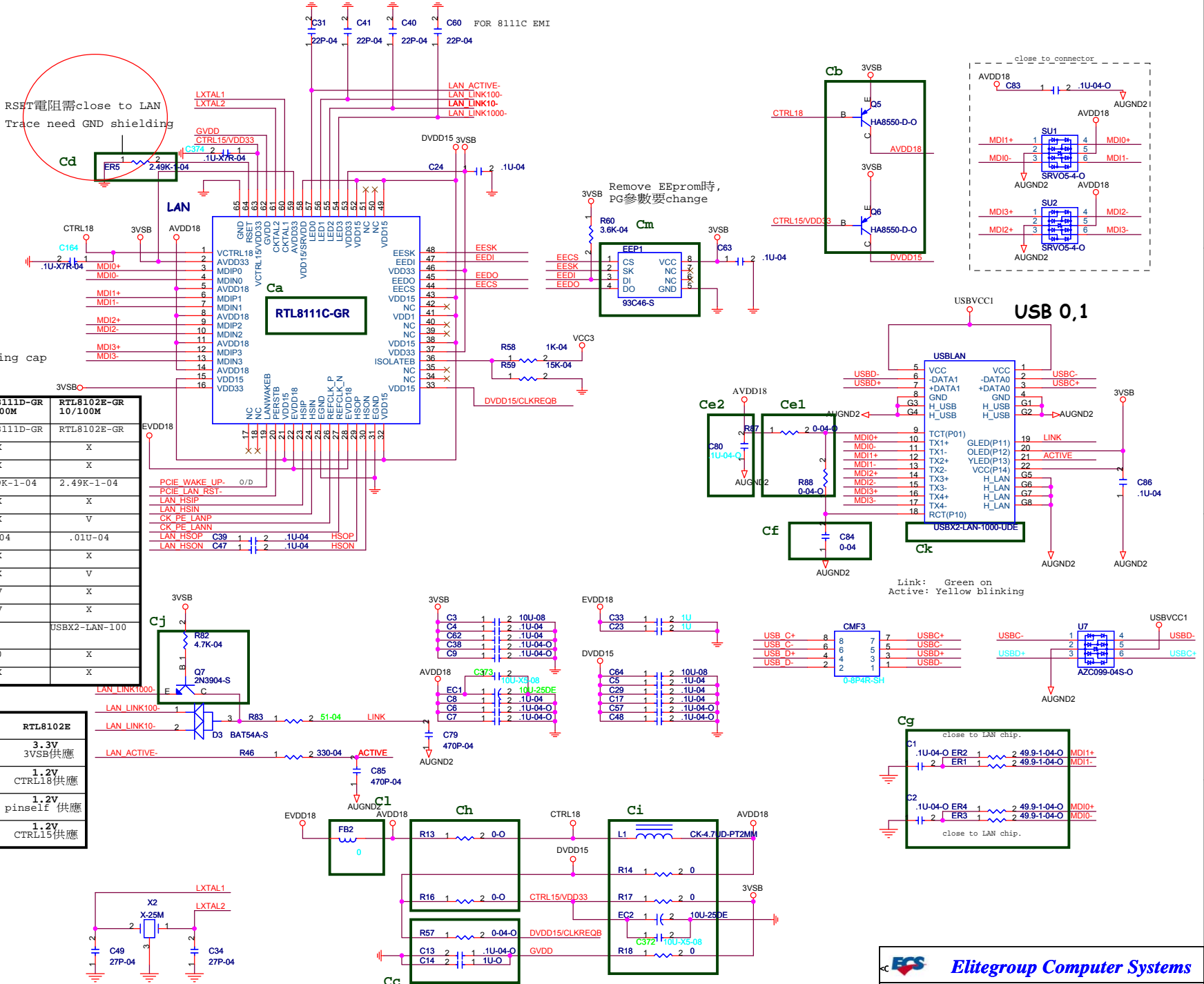
26 USB_P1+ USB C+

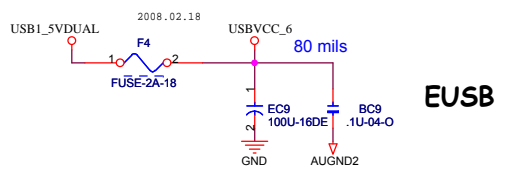
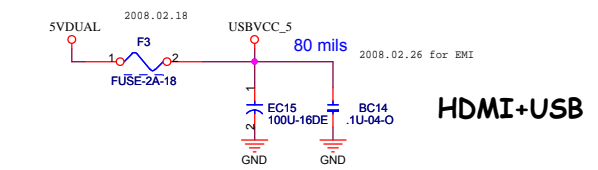
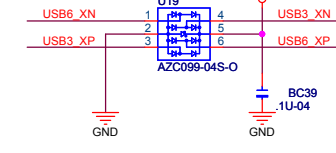
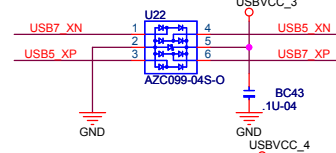
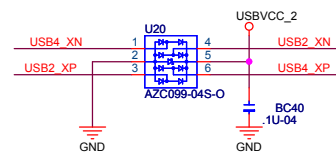
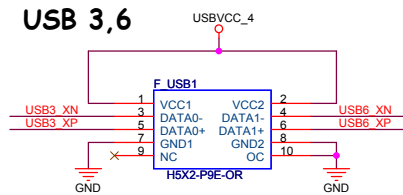
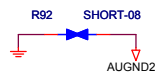
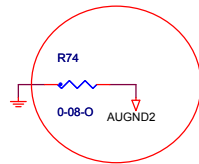
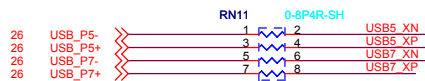
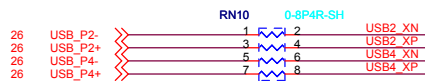
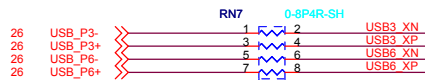
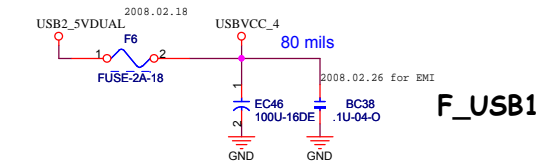
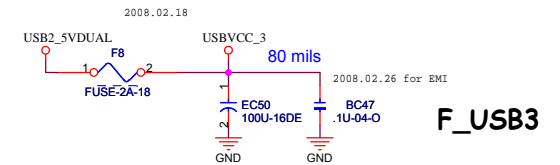
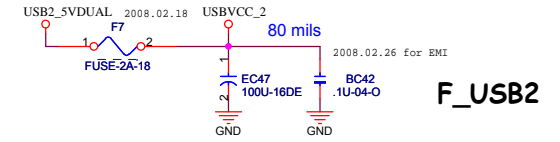
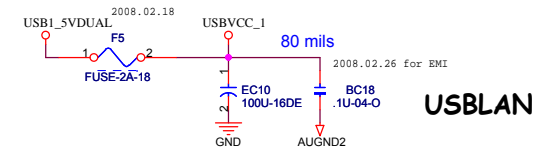
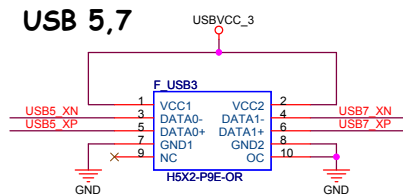
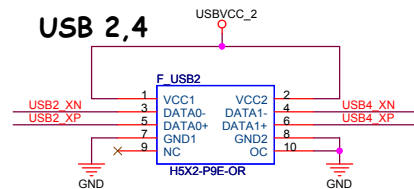
26 USB_P1- USB D+

26 USB_P1- USB D-

When you found some bug, please inform Ben(ext@e65) to update circuit.

N Difference				3VSB
RTL8101E-GR 10/100M	RTL8111B-GR 1000M	RTL8111C-GR 1000M	RTL8111D-GR 1000M	RTL8102E-GR 10/100M
RTL8101E-GR	RTL8111B-GR	RTL8111C-GR	RTL8111D-GR	RTL8102E-GR
X	V	X	X	X
V	V	X	X	X
2K-1-04	2.49K-1-04	2.49K-1-04	2.49K-1-04	2.49K-1-04
V	X	X	X	X
V	X	X	X	V
.01U-04	0-04	0-04	0-04	.01U-04
V	X	X	X	X
V	X	X	X	V
X	X	V	V	X
X	V	V	V	X
USBX2-LAN-100 symmetric	USBX2-LAN-1000			USBX2-LAN-100
0	0	0	0	X
V	V	V	X	X





External Connection

USB VCC₁ 6 VCC3 3 VCC3 3

AUGND2 2 AUGND2 2

17 GPP_TX3P PERx+
17 GPP_TX3N PERx-

17 GPP_RX3P PE1 IN
17 GPP_RX3N PE1 IN

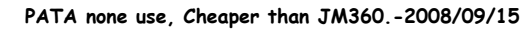
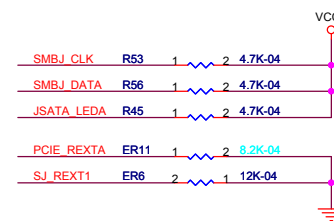
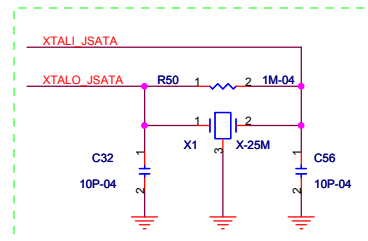
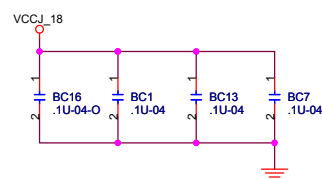
10 GB_CLK2P CK PE 100M SATA H
10 GB_CLK2N CK PE 100M SATA L

14,29 HDD_LED- HDDLED

31,34 -PCI1RST XRST_L

5,7,8,10,12,23,26,29,30 SMBCLK SMBCLK
5,7,8,10,12,23,26,29,30 SMBDT SMBDATA

26 USB_P10+ USB_C+1
26 USB_P10- USB_C-1
26 USB_P11+ USB_D+1
26 USB_P11- USB_D-1

[illegible]

		Elitegroup Computer Systems	
Title: [Micron eSATA-JM361]			
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ATX P/S WITH 1A STBY CURRENT				
5VSB +/-5%	5V +/-5%	3.3V +/-5%	12V +/-5%	-12V +/-5%

CPU PW
12V +/-5%

2.5V OP
REGULATOR

VRM (ISL6323)
REGULATOR FOR 140W

VCC_STR

RT9214

NB_1.8V OP

NB_1V8

RT9218

VCC1.1

VCC1.2

DDRII DIMMs
VTT_DDR 2A
VDD_MEM 12A

RT9173

V_DIMM

+2.5V_VDDA

VCC_CORE/CPU_VDDNB

DDR_VTT

V_DIMM

+1.2V_HT

AM3
VDDA 2.5V 0.2A
VDDCORE 0.8-1.55V 110A
DDRIII MEM I/F VTT 2A, VDD 10A
VLDT 1.2V 0.5A

RX780/RS780D
VDDHT/RX 1.1V 1.8A
VDDHT TX 1.2V 0.8A
NB CORE VDDC 1.1V7A
VDDPCIE 1.1V 3A
VDDA18PCIE 1.8V 0.9A
VDD18/VDDA18HTPLL VDDA18PCIEPLL 1.8V 0.6A
AVDD 3.3V 0.135A

SB700/750
X4 PCIE 0.8A
ATA I/O 0.2A
ATA PLL 0.01A
PCIE PVDD 80mA
SB CORE 0.6A
1.2V S5 PW 0.22A
3.3V S5 PW 0.01A
USB CORE I/O 0.2A
3.3V I/O 0.45A

AZALIA CODEC
3.3V CORE 0.3A
5V ANALOG 0.1A

SUPER I/O
+5V SD 0.01A
+5V 0.1A

eSATA
VCC3A_J(ASV33) 0.071A
VCCJ_18(DV18) 0.15A
VCC3(DV33) 0.045A
VCCA_J18(ASV18/APV18) 0.194A

PCIE_VDDR
AVDD_SATA
PLLVD_SATA
PCIE_PVDD
VCC1.2_SB
1.2VSB
3VSB
USB_PHY
VCC3

Jumper select

PCI Slot (per slot)
5V 5.0A
3.3V 7.6A
12V 0.5A
3.3Vaux 0.375A
-12V 0.1A

X1 PCIE
3.3V 3.0A
12V 0.5A
3VSB 0.1A

X16 PCIE
3.3V 3.0A
12V 5.5A

X16 PCIE
3.3V 3.0A
12V 5.5A

USB X4 FR
VDD 2.0A
5VDual 2.0A

USB X6 RL
VDD 2.0A
5VDual 2.0A

2XPS/2
5VDual 1.0A

RTL8111/8101E
3.3V 0.5A (S0, S1)
3.3V 0.1A (S3)


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DELIVERY CHART

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